ORDER NO. KMS9605142C2

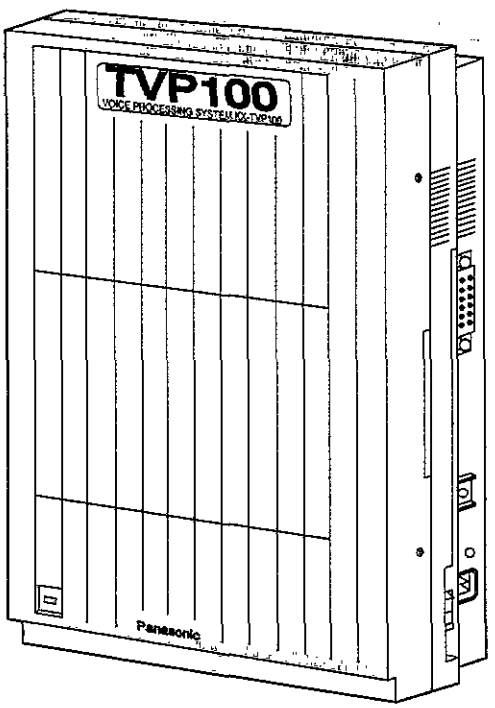
Service Manual

and Technical Guide

VOICE PROCESSING SYSTEM

KX-TVP100E

(for the United Kingdom)



⚠ WARNING

This service information is designed for experienced repair technicians only and is not designed for use by the general public.
It does not contain warnings or cautions to advise non-technical individuals of potential dangers in attempting to service a product.
Products powered by electricity should be serviced or repaired only by experienced professional technicians.
Any attempt to service or repair the product or products dealt with in this service information by anyone else could result in serious injury or death.

Panasonic

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When referring to the serial number, supply all 11 digits. The serial number may be found on the label affixed to the back of the unit.

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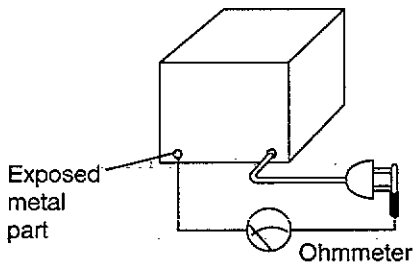
SAFETY PRECAUTIONS

1. Before servicing, unplug the power cord to prevent an electric shock.
2. When replacing parts, use only the manufacturer's recommended components for safety.
3. Check the condition of the power cord. Replace if wear or damage is evident.
4. After servicing, be sure to restore the lead dress, insulation barriers, insulation papers, shields, etc.
5. Before returning the serviced equipment to the customer, be sure to perform the following insulation resistance test to prevent the customer from being exposed to shock hazards.

INSULATION RESISTANCE TEST

1. Unplug the power cord and short the two prongs of the plug with a jumper wire.
2. Turn on the power switch.
3. Measure the resistance value with ohmmeter between the jumpered AC plug and each exposed metal cabinet part, such as screwheads, control shafts, handle brackets, etc.
   ***Note:** Some exposed parts may be isolated from the chassis by design. These will read infinity.
4. If the measurement is outside the specified limits, there is a possibility of shock hazard. The equipment should be repaired and rechecked before it is returned to the customer.



Resistance = more than 1 MΩ (at DC 500 V)

FOR SERVICE TECHNICIANS

ICs and LSIs are vulnerable to static electricity.
When repairing, the following precautions will help prevent recurring malfunctions.

1) Cover the plastic parts boxes with aluminum foil.
2) Ground the soldering irons.
3) Use a conductive mat on the worktable.
4) Do not touch IC or LSI pins with bare fingers.

Take special care when handling the Hard Disk Drive unit and KX-TVP100E.

SPECIFICATIONS

Ports :		2 to 4 SLT extensions, or D-PITS compatible
Dialing Method :		Tone duration/Pulse (10/20pps)
Flash time :		100/300/600/900 msec (programmable)
CPC Detection :		6.5/150/300/450/600 msec (programmable)
Type of line :		Loop start min Loop Current : 20 mA min Ringing Voltage : 40 Vrms
Extension numbering :		2 to 5 digits (programmable)
Pause time :		1 to 9 sec (programmable)
Message Waiting Lamp :		Programmable DTMF sequence, Data line of PITS interface
Main CPU :		16-bit microprocessor
Capacity for Hard Disk :		6 hours
Number of Mailboxes :		Max. 64
Number of Messages :		Max. 100 per mailbox (programmable)
Personal Greeting Message Length :		8 to 60 sec (programmable)
Message Retention Time :		1 to 30 days, or unlimited (programmable)
Maximum Message Length :		1 to 6 min. (programmable)
Reports :		Mailbox List, Class of Service List, System Service Report, Call Account Report, Port Usage Report, Mailbox Usage Report, FAX Report
Connections	Telephone line :	Modular connectors × 2 2-conductor wire × 1 4-conductor wire with DPITS interface × 1
	Data port :	RS-232C interface port
Power Source :		AC 230-240 V, 50 Hz
Dimensions (H × W × D):		468 × 327 × 101 mm (18-7/16" × 12-7/8" × 4")
Weight:		6.2 Kg (15 lb 7 oz)

OVER VIEW

This chapter describes the hardware overview of the Voice Processing System (VPS).

1. SYSTEM OUTLINE

The Panasonic Voice Processing System (VPS) is a voice prompted, menu-driven system which provides fully automated call transfer (to an extension or mailbox), and voice message receiving and delivery service. Even firsttime users can easily reach their desired extension or mailbox by following step-by-step voice instructions. The VPS works with a PBX as an extension. It can be expanded to handle up to four simultaneous calls and store up to four hours of voice data.

The VPS attends to incoming calls, then transfers those calls to the respective extensions. When owners of extensions cannot answer the call, the mailboxes in the system take messages for them. Owners of the mailboxes can record personal greeting messages with their own voice for callers who enter the mailbox to leave messages.

The VPS has up to 62 personal mailboxes for subscribers and two special function mailboxes for the System Manager and Message Manager.

The VPS can be used by any caller, and by subscribers (Mailbox Owner) in your company.

Even if the user is away from the office, VPS can be used with any touch tone telephone.

Even callers using a rotary telephone can leave messages or be connected with the operator.

The VPS provides the following incoming call services to callers.

1-1. Automated Attendant (A.A.) Service

The automated Attendant works as a receptionist would by answering incoming calls without human intervention.

The Automated Attendant plays a list of options (calling extension, calling operator, Department Dialing, Dialling by Name) to a caller with a voice prompt. When an option has been selected, the Automated Attendant responds to the command by either routing the caller to an extension or the operator. The Automated Attendant will even respond if the extension is busy or if there is no answer.

One option is to let the caller leave a message in a mail box.

1-2. Voice Mail (V.M.) Service

Voice Mail is a voice message receiving and delivery service which allows subscribers (the owner of a personal mailbox) to receive messages in their mail box whether they are out of the office, on the line, or just unavailable to answer the call.

Any caller can leave a message in a subscriber's mailbox. The subscriber can listen, transfer, and deliver recorded messages at any time from anywhere in the world.

1-3. Interview Service

You can set up a questionnaire mailbox with as many as 10 questions, and obtain specific information from customers calling into the system. Between each recorded question, the VPS collects a reply from the caller and stores it in a mailbox.

This service is ideal for gathering any data from product orders to requests for repairs.

1-4 Custom Service

The Custom Service capability optimizes the application of the VPS to meet your business needs. Your callers can access the services or people they need by pressing a single digit on their telephone keypad.

As many as two custom service scripts can be assigned to each VPS port (Day Service and Night Service).

2. SYSTEM PROGRAMMING

This system can be programmed either by a data terminal (VT100, compatibles, or other ASCII terminals) through the System Administrator Interface or by telephone (touch tone telephone) through the System Manager mailbox.

2-1. Terminal Based Programming

After system installation, it is recommended that you perform "Quick Setup" first.

<Quick Setup>

Provides a fast way of setting up the VPS for basic Voice Mail or Automated Attendant service. This includes mailbox creation, incoming call service assignment for all ports, time setting and several other programming items which must be done initially to start the VPS operation.

<PBX Integration>

The VPS is a 2-port system. Typically, each VPS port is connected to an extension port of the PBX. Between PBX's, the VPS exchanges a request to a counterparty or status for itself mutually, then offers a quick and useful service. The VPS works well with all Panasonic KX-T series PBX's and can be programmed to work with most other manufacturer's PBX's that fully support single line telephone interfaces.
However, because the VPS operation depends on the capabilities and features provided by the PBX, its performance will vary when connected to different PBX's. In system program, Integration Parameter with a PBX should be installed to achieve quicker and more useful service.

2-2. Telephone Based Programming

During daily operation, the person specified as the System Manager can create and/or delete mailboxes, and change Class of Service parameters.

3. SYSTEM CONFIGURATIONS

The most common configuration of the VPS is behind a PBX. The VPS ports are connected to PBX extension ports.

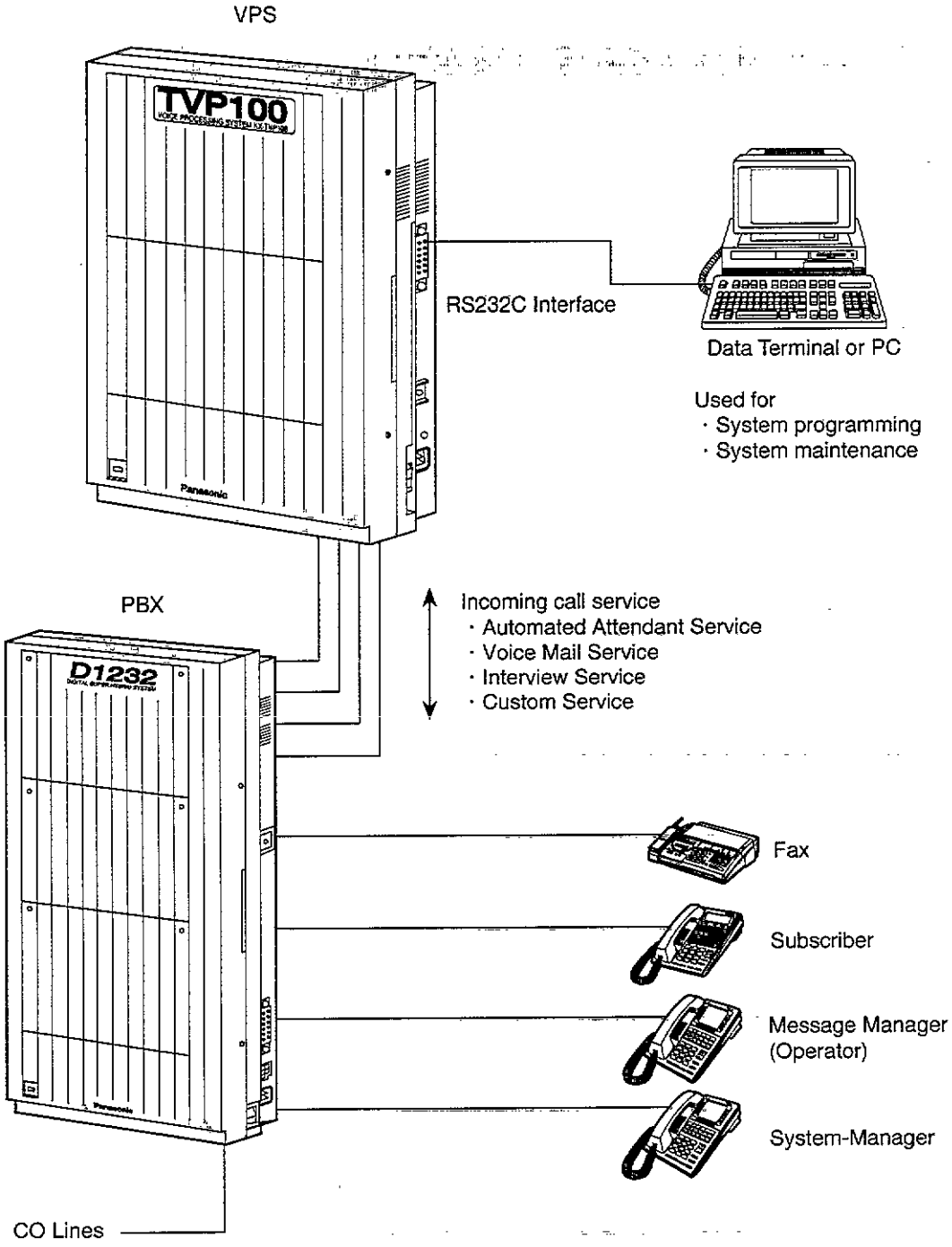


Fig. 1-1. Typical Configurations

4. SYSTEM COMPONENTS

4-1. Outside Equipment

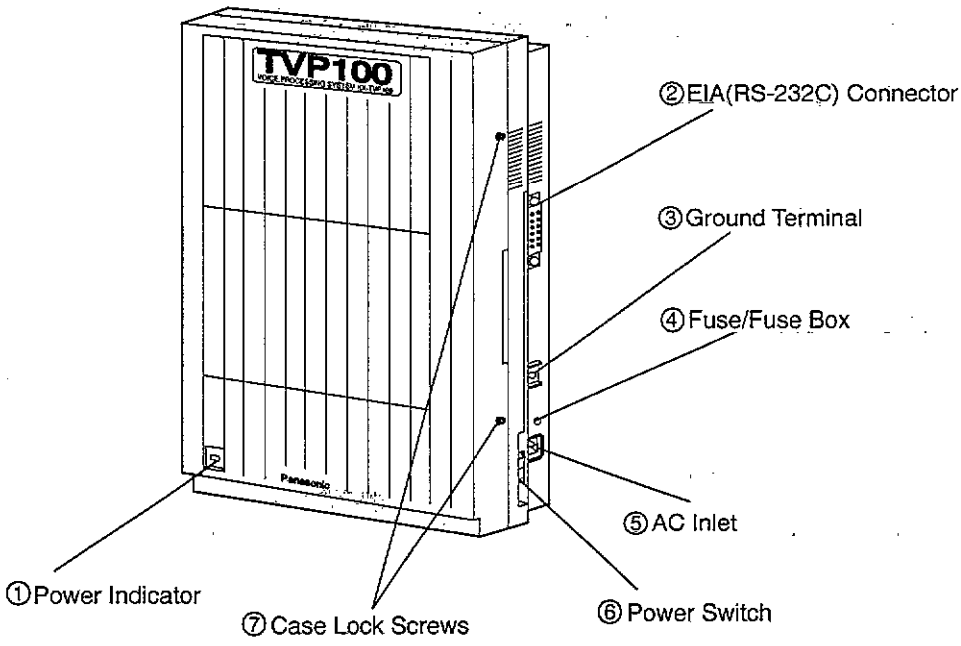


Fig. 1-2. Cabinet Outside View and Equipment Location

①Power Indicator

Power Indicator indicates VPS status. When you turn on the power switch, the power indicator turns on. During this period, the VPS exexutes self diagnostics. When the self diagnostics finishes normally, this indicator starts the blinking sequence. During this period, the VPS executes the system initialization. When this initialization finishes normally, the indicator lights on again, and the VPS stsrts the incoming service. When the VPS detects any error on system, the Indicator informs the type of error by using a specific blinking sequnce.

②EIA (RS232C) Connector

The VPS allows to communicate with a Data Terminal or with any standard ASCII Terminal for system programming. The terminal is connected to the VPS using an RS232C cross cable. Attach the 25-pin connector to the jack marked "RS-232C" on VPS.

③Ground Terminal

Ground Terminal is an earth terminal.
Tie the ground line to the Ground Terminal marked "GROUND" on the VPS.

④Fuse/Fuse Box

This fuse is a safety part for AC power line. In order to use the VPS safely, it is required to use a regulated fuse indicated on the label.

⑤AC Inlet

AC inlet is an input connector of AC power source. Attach AC power code to AC Inlet marked "AC IN" on the VPS.

⑥Power Switch

Turn the power switch on the side of marked "ON", then AC Power is supplied to the VPS.
Turn the power switch on the side of marked "OFF", then supply of AC Power is cut.

⑦Case Lock Screws

The VPS has two case lock screws to open the front cover.

4-2. Inside Components

Inside of the VPS is covered by two pieces cabinet. These two cabinets are fixed to the base cabinet with two and four screws.

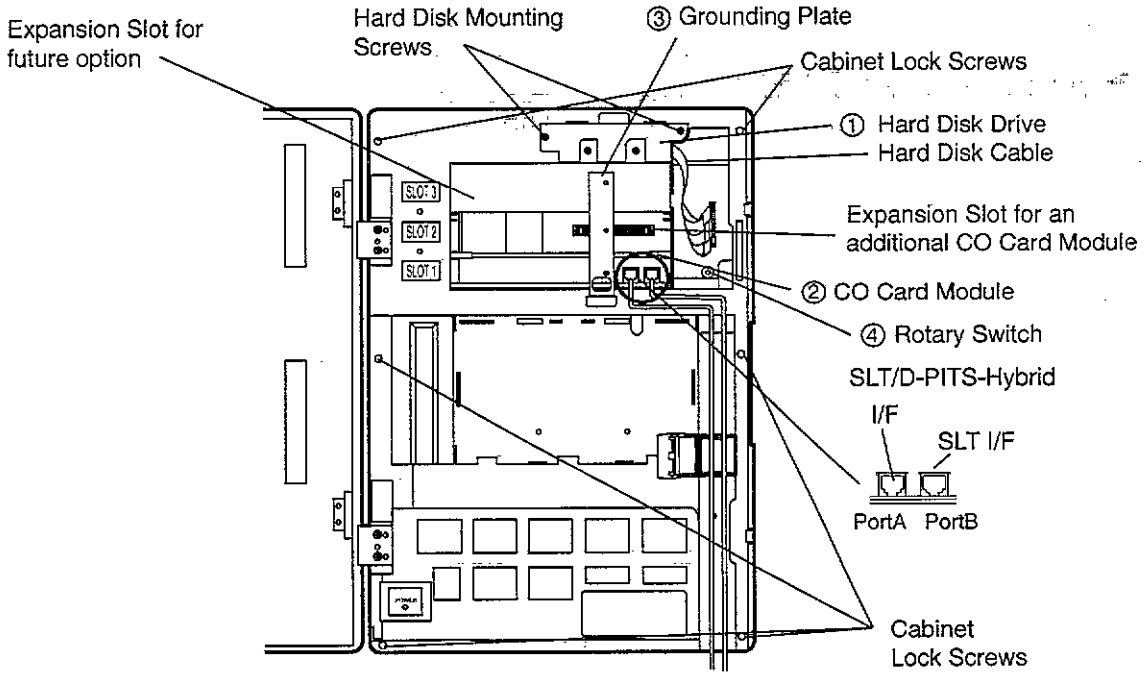


Fig. 1-3. Inside View and Components Location

① Hard Disk Drive (HDD)

The Hard Disk Drive (HDD) is installed Proprietary System Program and System Prompt. All the recorded messages from callers are stored in the HDD. The HDD is connected to CPU card using a 44-pin flat cable.

②CO Card Module

CO Card Module, composed by COL Card and DSP Card, has two Single Line Telephone (SLT) interface with one card. Port-A is Hybrid interface, providing interface with Panasonic KX-TD series PBXes Proprietary digital Extension Line (D-PITS). COL card possesses SLT/DPITS interface, changes voice region data to digital. DSP Card plays back registered messages and prompt in HDD and records incoming messages.

③Grounding Plate

This Grounding Plate is an earth plate. To protect the printed circuit board from static electricity, first dischange any body static by touching the grounding plate.

④Rotary Switch

The Rotary Switch Provides additional function as follows. The status of this switch is checked only once after power-up. The additional functions are effective when you turn on the power after the switch changing.

Position	additional function
0	Normal Operation
1	The VPS automatically sets the RS-232C baud rate to the following parameters: baud rate 9,600 bps bit length 8 bit stop bit length 1 bit parity None In this case, the communication parameter which was programmed by the customor is ignored.
2~4	Reserved for future function.
5	The VPS initializes all of the configuration settings to default setting, and clear all of the stored messages.
6~9	Reserved for future function.

4-3. Basic Components

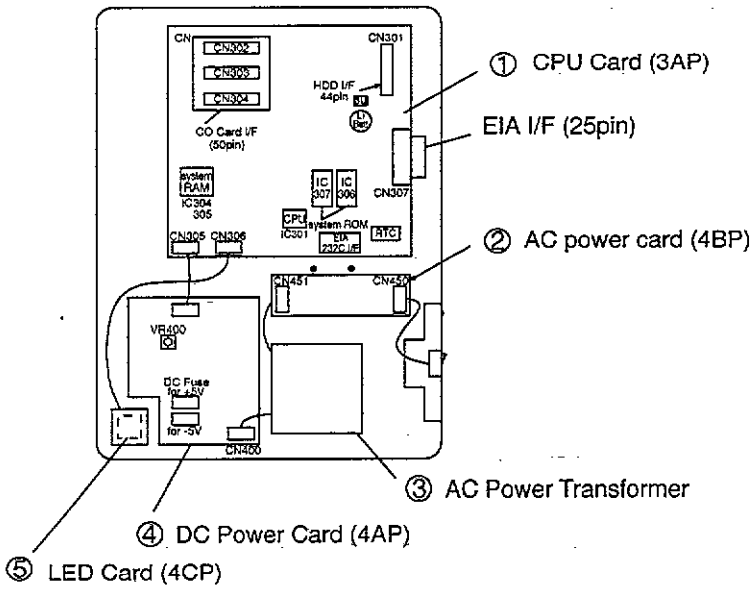


Fig. 1-4. Basic Components Location

Basic Components of VPS are CPU card, Power Card and AC Transformer. (Refer to Figure 1 - 4.)

①CPU Card (3AP)

The CPU Card is the central processing unit of the VPS. When power is on, the microprocessor (IC301) on the CPU Card runs on the ROM (IC306, 307) based program, and executes the system initialize, self diagnostics and then an application program loading from HDD to system RAM on the CPU Card. After the program loading, CPU Card starts the incoming call service. The CPU Card allows to control the EIA232C interface and the real time clock device with back up battery. The CPU Card has 7 interface connectors as follows.

CN301 = HDD interface (44pin)
CN302 ~ CN304 =CO Card interface (50pin)
CN305 = DC power supply from power card (8pin)
CN306 = Power Indicator (LED) interface (2pin)
CN307 = EIA232C interface (25pin)

②AC Power Card (4BP)

The AC power source inputs from AC inlet to Power card (4BP) via CN450.

The Power Card (4BP) has the AC line filter and the surge protector logic. The 4 BP is closed in the box to prevent electric shock to a maintenance user. The AC power source outputs to the transformer from the 4BP via CN451.

③AC Power Transformer

AC Power Transformer works as follows.
•Isolate DC Power logic from AC line.
•Drop AC Power level, then supplies to DC power logic. Over current temperature fuse is installed in this transformer.
The transformed AC power output to DC Power Cord (4AP) via CN400.

④ DC Power Card (4AP)

Power Source inputted from AC Transformer is rectified in DC Power Card, and then changed to DC +5V and to DC-5V. Functions of DC Power Card is as follows.
•DC±5V generation.
•DC+5V back up by using large capacity capacitor.
•Power down detection.
•DC shut down control in case of abnormal condition of the voltage, current and temperature.
This DC Power card (4AP) has a variable resister (VR400) for +5V DC voltage adjustment.
DC Fuses for protection are F400 for + 5V and F401 for -5V.
DC power source generated in Power logic is supplied to CPU card via CN401.

⑤LED Card (4CP)

LED Card is connected to CPU Card via CN306 and its ON/OFF states are controlled by the CPU Card.

4-4. Hardware Architecture Outline

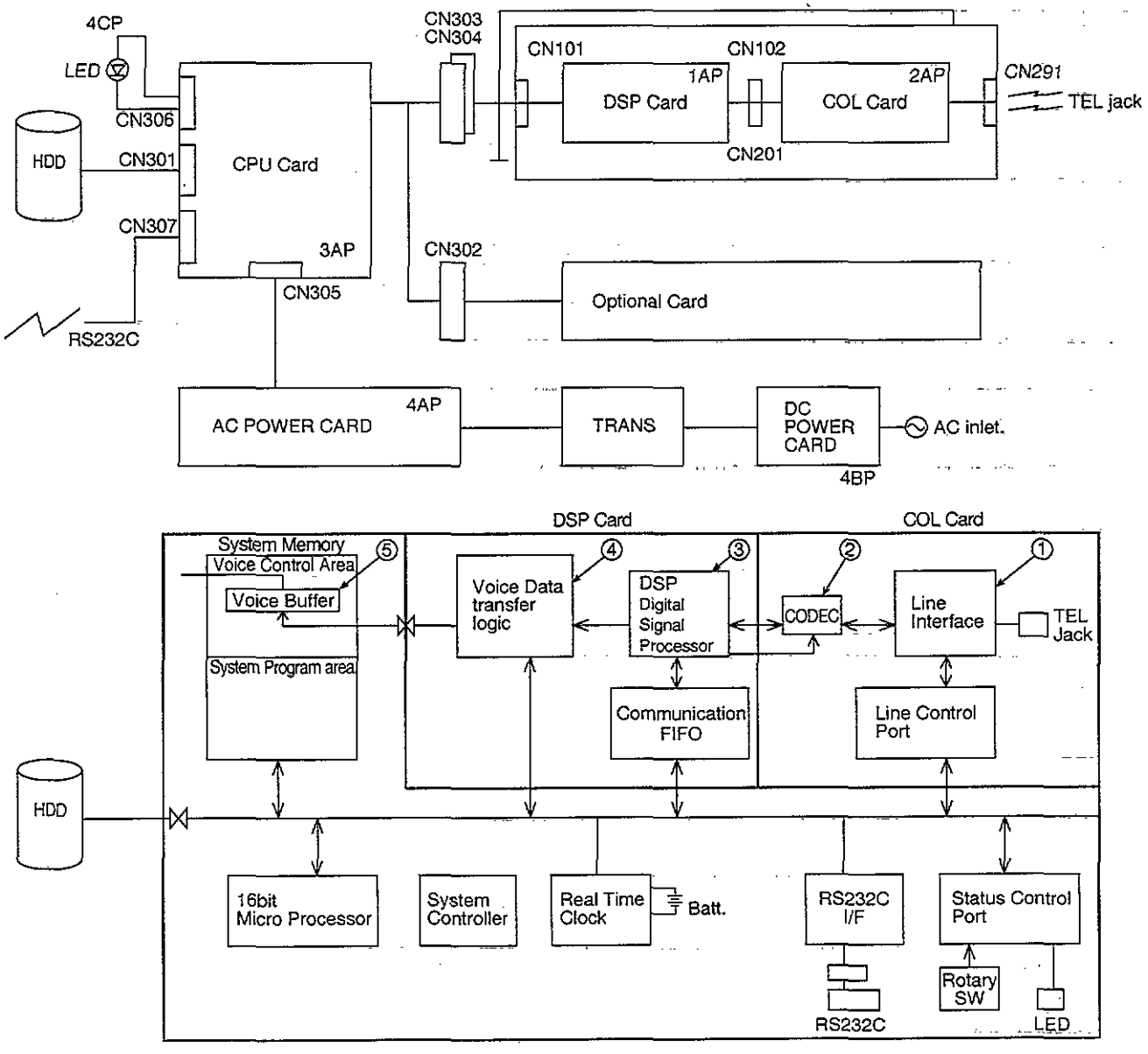


Fig. 1-5. Hardware Block Diagram

A Hardware block diagram of the VPS is shown in figure 1 - 5.
Functions of each hardware block are explained by giving an example of the process from guidance play back to message recording by Voice Mail Service.

•Bell arrival

Line interface has a function to detect the bell signal inputted from Tel Jack. The 16 bit Microprocessor monitors this bell arrival through the Line Control Port periodically. When the 16 bit Microprocessor detects the bell arrival, the Microprocessor makes the line condition into an off-hook state through the line control port.

•Guidance Play back

At the same time the Microprocessor transfers system prompt data stored in the HDD in advance from HDD to a voice buffer area in the system memory. (This system prompt data is compressed in half by ADPCM algorithm) The Microprocessor programs the Voice Transfer logic to the play back mode. In addition, the Microprocessor writes the play back command into FIFO on the DSP Card. DSP monitors this FIFO periodically. If DSP receives a playback command by FIFO monitoring, DSP starts to execute ADPCM play back. In ADPCM play back the following processes are executed.

System prompt data, transfered from system memory by the voice data transfer logic , is encoded to digital voice data, then output to CODEC. The CODEC converts digital voice data to analog voice data, and outputs to the line interface. In ADPCM play back mode, the DTMF detecting function is always activated and checks reception of the DTMF code by DSP.

•Message Recording

When DSP detects a DTMF code represented recording, it writes the DTMF code into FIFO. Microprocessor monitors this FIFO periodically. The Microprocessor receives DTMF code represented recording messages intermittently, then the Microprocessor programs Voice Data Transfer logic to Recording mode. The Message recording command is written into FIFO on the DSP card. DSP receives message recording command intermittently, DSP starts to execute ADPCM recording . In ADPCM recording, the following processes are executed. Voice data input from the line interface is converted to digital voice data by CODEC. DSP receives digital voice data from CODEC and executes the voice data compression based on ADPCM algorithm. DSP outputs the compressed data to Voice data transfer logic. Voice data transfer logic transmits the compressed data from DSP to system memory. Data transferred to system memory is stored in HDD by the Microprocessor. In ADPCM recording mode, DTMF detecting function, Tone detecting function, and VOX (silence) detecting function are always activated by DSP. The result of this detection is written into FIFO by DSP periodically.

•End of Message Recording disposition

The Microprocessor receives these detection results via FIFO, then detects the recording termination. (For example the conditions of termination are to receive the DTMF code representing recording finish, detect a Busy Tone or a detected silence situation more than a regulated period, etc.) When the Microprocessor detects a recording, it terminates the recording disposition then shifts over to the next step, guidance play back disposition.

The functions of the module are as follows.

•HDD	to store the voice data, and the system program.
•System memory	to store voice data temporarily, to execute the system program.
•Voice Data Transfer logic	to control the transfer of voice data between DSP to/from system memory
•DSP	voice compression/decompression (using ADPCM Algorithm).
	to detect and generate DTMF.
	to detect Tone and generate Beep Tone.
	to detect VOX (silence).
	to adjust recording level. (Automatic Recording Level Control)
•Codec	Analog to/from digital conversion of the voice data.
•Microprocessor	controls all of the system.

INSTALLATION

1. INSTALLATION REQUIREMENTS

The VPS installation involves
- Mounting the VPS.
- Connecting PBX extensions to the VPS ports.
- Connecting a Data Terminal (VT or ASCII)
- Connecting Power to the Cabinet.
- System Programming (→ Refer to Installation Manual)

Installation personnel should be familiar with the data format and change procedures of the PBX. For further explanation, refer to the "Installation Manual".

1-1. Site Requirements

Install the VPS cabinet in a dust free location. Keep it separated from other equipment that may produce heat or generate strong magnetic fields. If space permits, install the VPS in a telephone equiment room.

1-2. AC Power Requirement

It is best to power the system from a dedicated, separate circuit. If this is not possible, make sure the circuit is free of large motorized equipment, such as copy machines, and that it is protected by a fuse or circuit breaker. Make sure the power receptacle is grounded and within five feet of the cabinet.

1-3. Other Required Equipment

Each VPS port is connected via a modular line cord to a standard modular telephone jack connected to a PBX extension. Each line cord must be of sufficient length to reach between the VPS and PBX without undue stretching or tension. Keep it separated from other cords that may generate strong electric magnetic wave.
A data terminal, used for system programing, must be available at the customer site. In addition, one RS-232C cross cable is required to connect the terminal to the VPS.

The following is a list of required equipment.

Table 1-1, Installation required equipment.

Modular line Cord (male-male)	4 wire	1 cord/2 port (when connecting Panasonic KX-TD Series PBX extension)
	2 wire	1 cord/1 port (when connecting other type PBX extension)
Data Terminal (VT or ASCII)	1	
RS232C Cross Cable	1	
Screw Driver	1	
Drill	1	

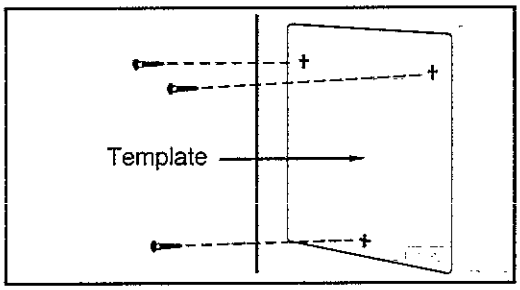
2. MOUNTING THE VPS

Mounting the VPS on the Wall

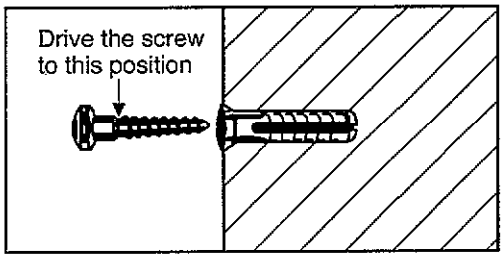
The wall where the VPS is to be mounted must be able to support the weight of the VPS. If screws other than the ones supplied are used, use the same-sized diameter screws as the enclosed ones.

To Mount on a Wooden Wall:

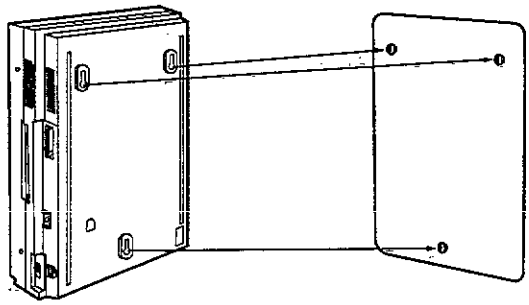
1) Place the template (included) on the wall to mark the 3 screw positions.



2) Install the 3 screws into the wall.

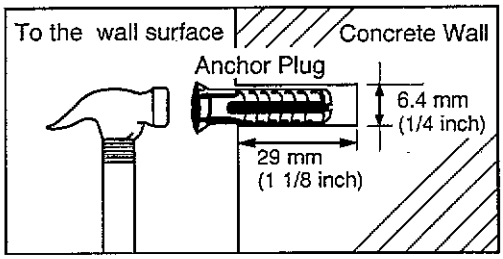


3) Hook the unit on the screw heads.

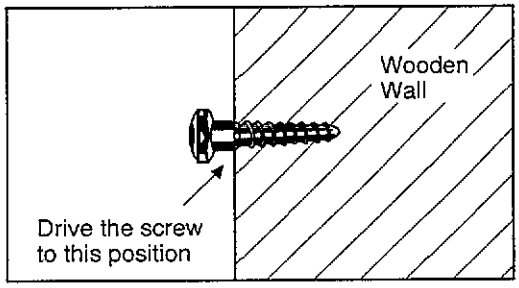


To Mount on Concrete or Mortar Walls:

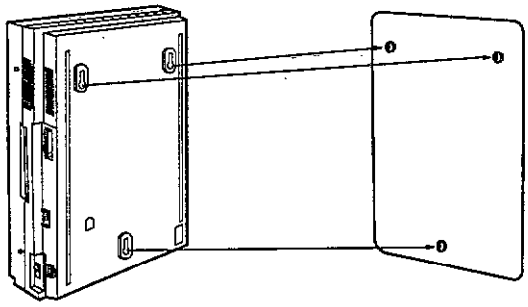
1) Place the template (included) on the wall to mark the 3 screws positions.
2) Drill 3 holes and drive the anchor plugs (included) with a hammer, flush to the wall.



3) Install the 3 screws into the anchor plugs.



4) Hook the unit on the screw heads.



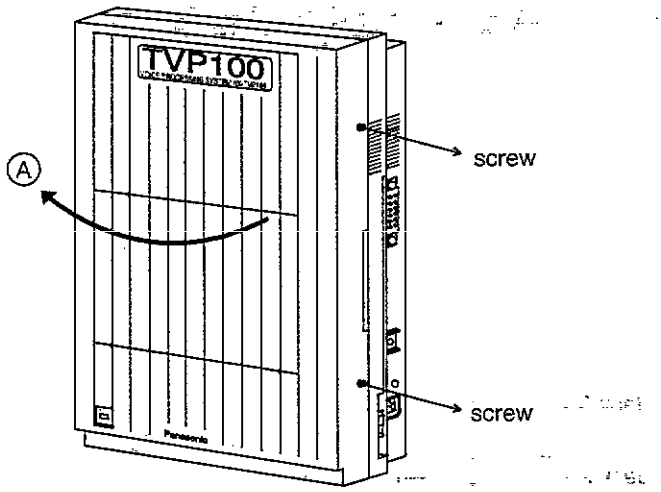
3. CONNECTING THE PBX EXTENSIONS TO THE VPS

The VPS must be connected to PBX extension lines. If you have a Panasonic KX-TD series PBX and make use of D-PITS Integration, use a 4 conductor wiring cord. If you have another type PBX, use a 2 conductor wiring cord. The maximum length of the wire varies according to your PBX type. Please refer to your PBX Installation Manual. Remember the connected extension port number on the PBX. You will call it when accessing one of the assigned incoming call services. The following models are recommended for connecting to the VPS:

- Panasonic KX-T30810
- Panasonic KX-T61610
- Panasonic KX-T123210
- Panasonic KX-TD816
- Panasonic KX-TD1232

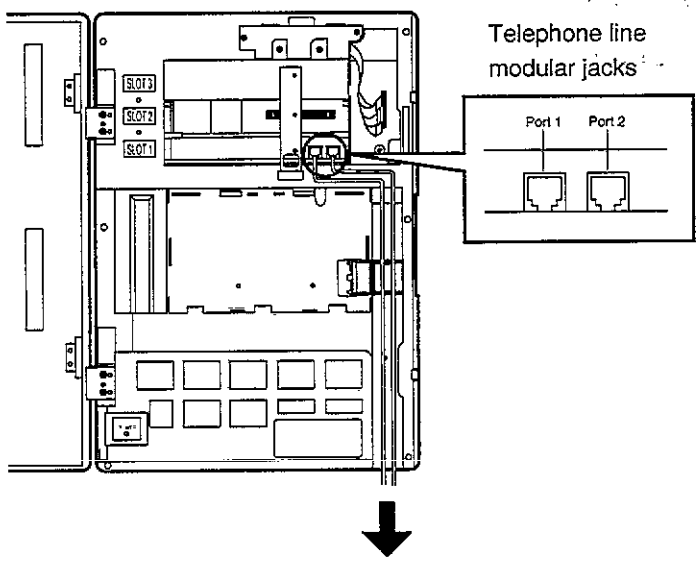
Procedure

1. Loosen two screws on the right side of the main unit, then open the front cover in the direction of arrow Ⓐ.



Note: The screws are attached to the front cover with springs so that they will not be lost.

2. Insert the modular plug of the telephone line into the modular jack on the CO Card.



To extension port of the PBX

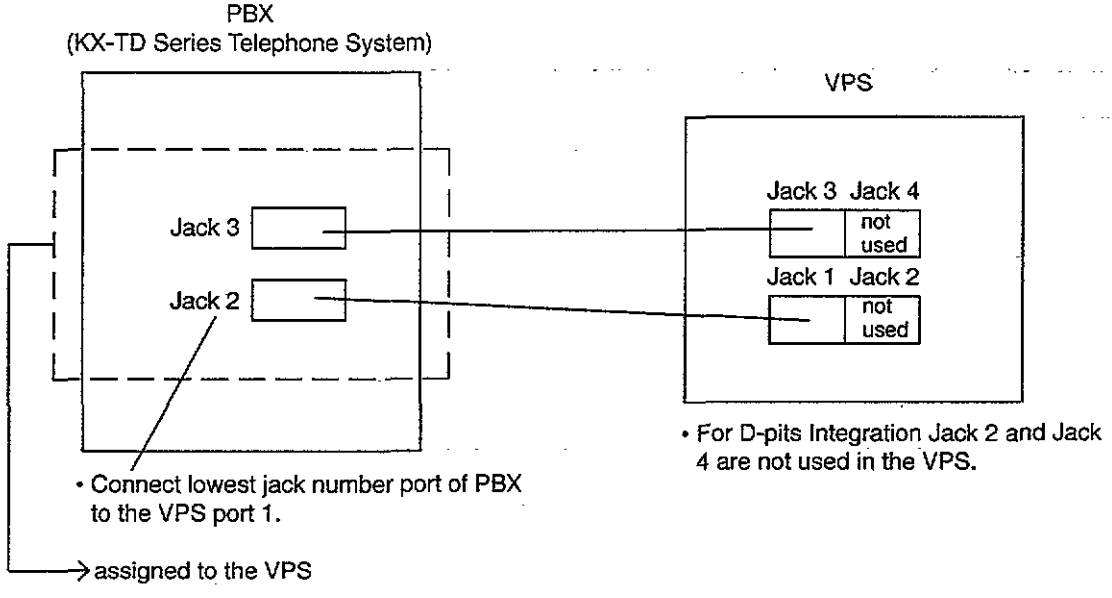
Notes:•Make sure the telephone cord is connected to the proper modular jack. Modular jacks on the Port Card correspond to the port numbers as follows:

SLOT #	Modular Jack	Port Number
1	Left	1
1	Right	2
2	Left	3
2	Right	4

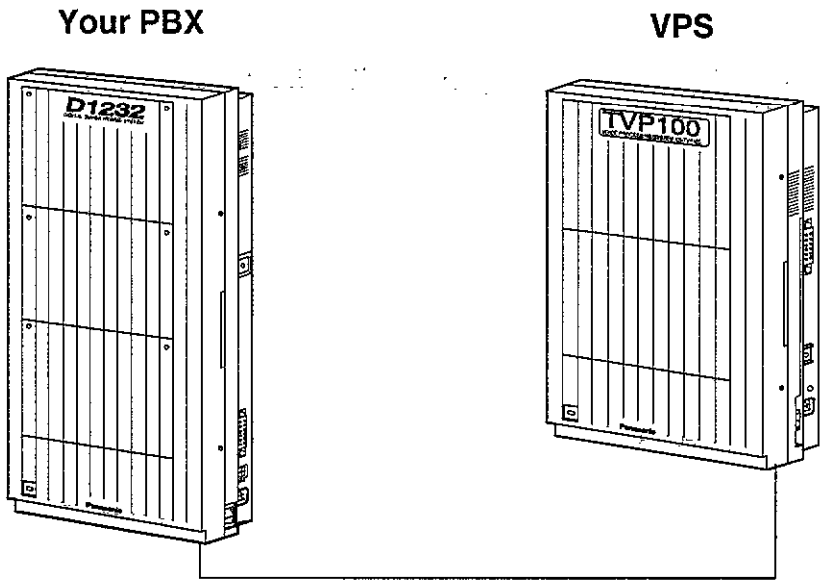
You can assign one of the incoming call services according to the port number.

Check : Connecting between the VPS and the Panasonic KX-TD series PBX with D-PITS integration.
To utilize D-PITS Integration
- Make sure to connect the Port 1 of the VPS to the lowest number jack of the PBX extensions.
- For D-PITS integration, the extension line interface allow to share a wire between Port 1 data and Port 2 data. (Port 3) (Port 4)

Example: Connecting to the KX-TD series PBX.



3. Connect the telephone line to the extension port of the PBX by following instructions below.



4. Close the front cover of the VPS system (and PBX if the cover is removed).
   Reverse the procedure of step 1.
5. Tighten the two screw firmly.
   Reverse the procedure of step 1.

4. CONNECTING A DATA TERMINAL

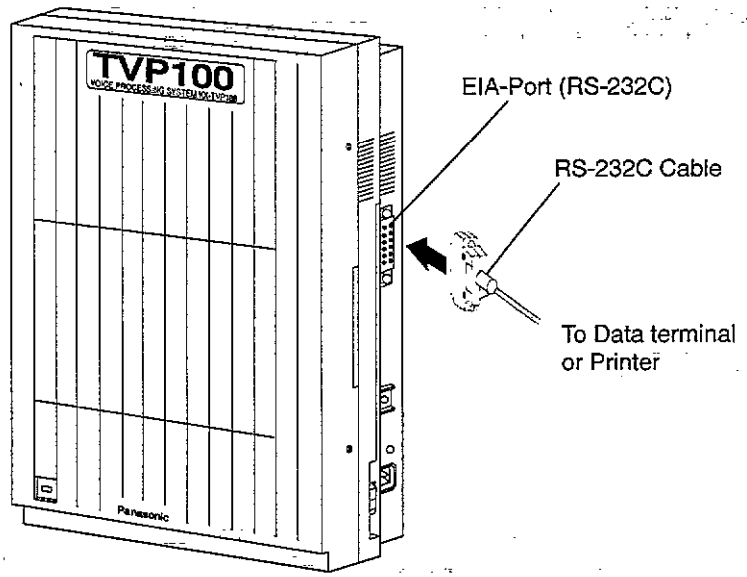
For the system administration (system set-up, mailbox setup, and system diagnosis), the VT 100 or ASCII terminal must be connected to a serial interface (EIA port) of the VPS. If using DEC VT100 or VT100 compatible terminal, the system administrator program provides the conversational menu-driven environment. If you wish to output reports to a printer, also connect to the VPS and the printer using the EIA port. The wiring and parameters are the same as those for a terminal. The default communication parameters of the VPS are shown as follows.

RS-232C parameters

- Baud Rate: 9600 bps
- Word Bit Length: 8 bits
- Parity: None
- Stop Bit Length: 1 bit

Connecting RS-232C cable

Precaution Before connecting the cable, make sure to turn off the power switch on both data terminals and the VPS.



1. Attach the 25-pin connector of cable to the jack on the VPS.

Note: Printer Connection

1. Make cables so that the printer may be connected to the VPS as shown in the following chart. Shielded cable is required and keep the length to less than 2m (6.5 feet).

Connection Chart:

EIA (RS-232C) port on the VPS			EIA (RS-232C) port on the Printer		
Circuit Type (EIA)	Signal Name	Pin No.	Pin No.	Signal Name	Circuit Type (EIA)
AA	FG	1	1	FG	AA
BA	TXD	2	3	RXD	BB
BB	RXD	3	2	TXD	BA
CC	DSR	6	20	DTR	CD
AB	SG	7	7	SG	AB
CD	DTR	20	5	CTS	CB
			6	DSR	CC
			8	DCD	CF

The pin configuration of the EIA (RS-232C) connector is as follows.

Pin No.	Signal Name		Circuit Type	
			EIA	CCITT
1	FG	Frame Ground	AA	101
2	TXD	Transmitted Data	BA	103
3	RXD	Received Data	BB	104
			CA	105
6	DSR	Data Set Ready	CC	107
7	SG	Signal Ground	AB	102
			CF	109
20	DTR	Data Terminal Ready	CD	108.2

(Reference)
EIA (RS-232C)
SIGNALS

Frame Ground (FG)
Connects to the unit frame and the earth ground conductor of the AC power cord.

Transmitted Data (TXD) ..... (output)
Conveys signals from the unit to the printer (or terminal). A "Mark" condition is held unless data or BREAK signals are being transmitted.

Received Data (RXD) ..... (input)
Conveys signals from the printer (or terminal).

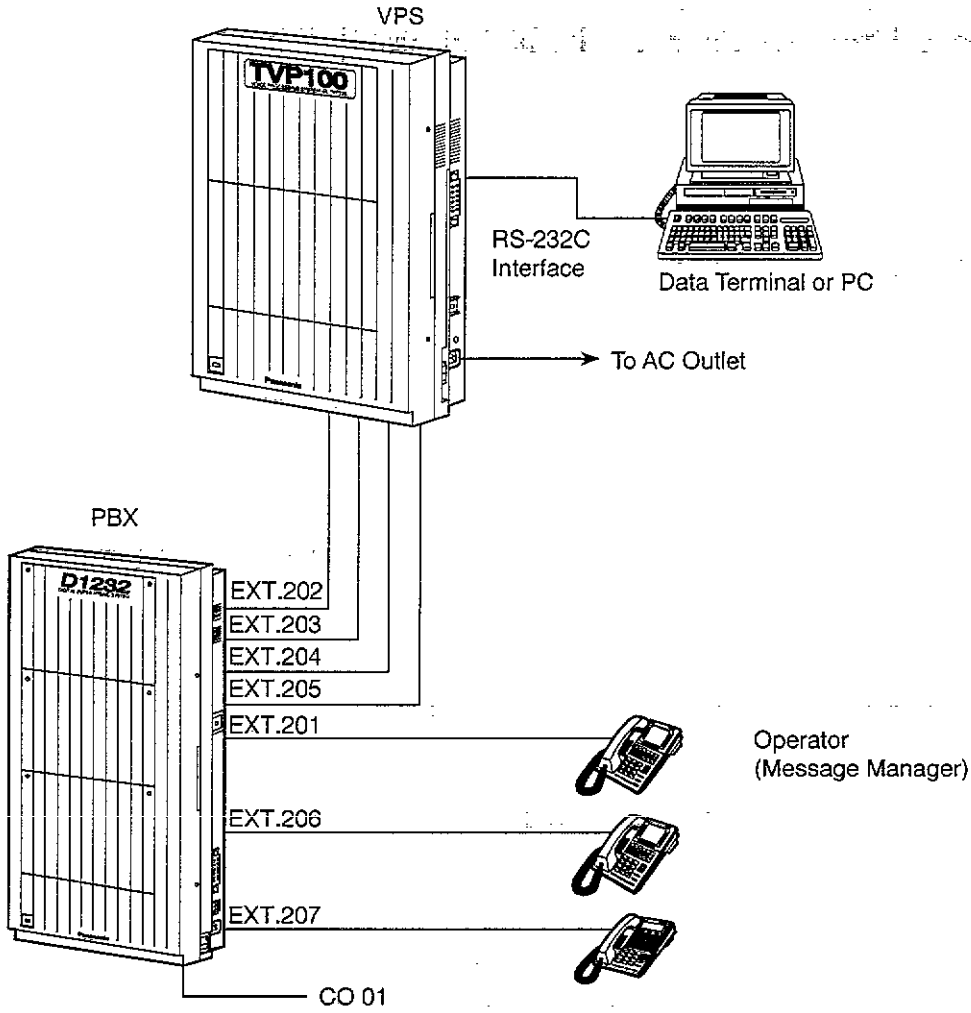
Data Set Ready (DSR) ..... (input)
An ON condition of circuit DSR indicates the printer (or terminal) is ready. Circuit DSR ON does not indicate that communication has been established with the printer.

Signal Ground (SG)
Connects to the DC ground of the unit for all interface signals.

Data Terminal Ready (DTR) ..... (output)
This signal line is turned ON by the unit to indicate that it is ON LINE. Circuit DTR ON does not indicate that communication has been established with the printer (or terminal). It is switched OFF when the unit is OFF LINE.

5. CONNECTING POWER TO THE CABINET

Attach the AC jack at the cord to AC inlet of the VPS.
Before connecting the power cord to an AC outlet, make sure all other connections (RS-232C data terminal with VPS, PBX with VPS, PBX with telephone lines) are correct. Attach the AC jack to AC outlet and then turn on the power switch.



6. SYSTEM PROGRAMMING

For the details of the system programming, refer to "Installation Manual".

7. STARTING THE SYSTEM

Turn on the power switch, the VPS will start up in the following sequence.

<Screen on the Terminal>

```
CARD TEST...

SYSTEM SETUP...

1.. 2.. 3.. 4..

ACTIVE COs : 1, 2


** ON LINE MODE

>
```

<Procedure>

Self diagnostics
(LED ON)

↓

System initialize
(LED BLINK)

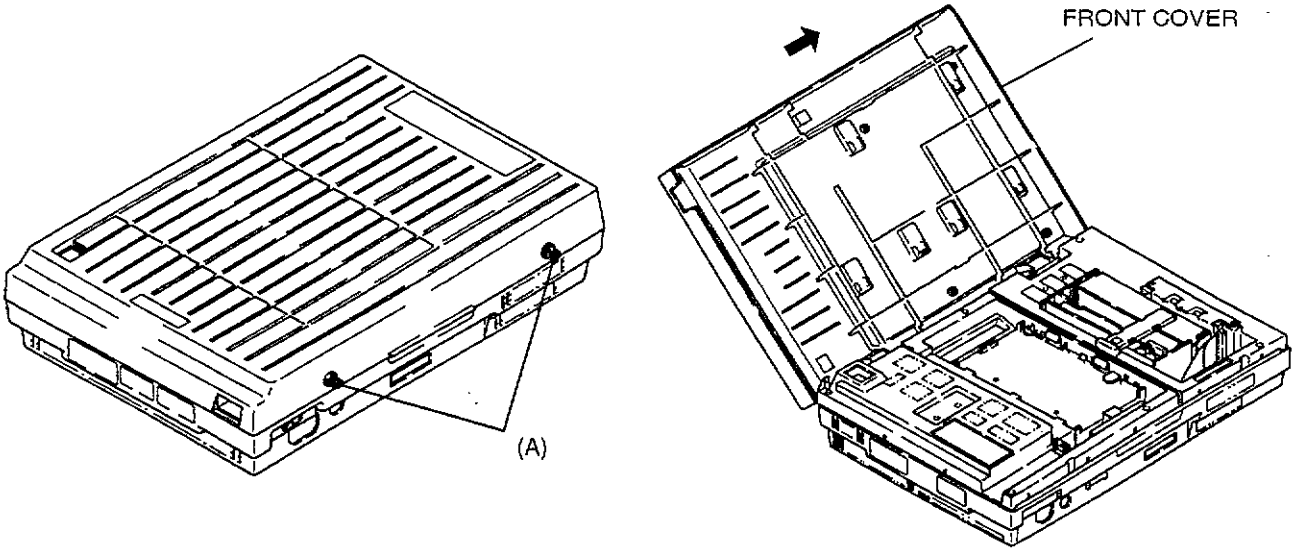
↓

operation mode
(LED ON)

DISASSEMBLY INSTRUCTIONS

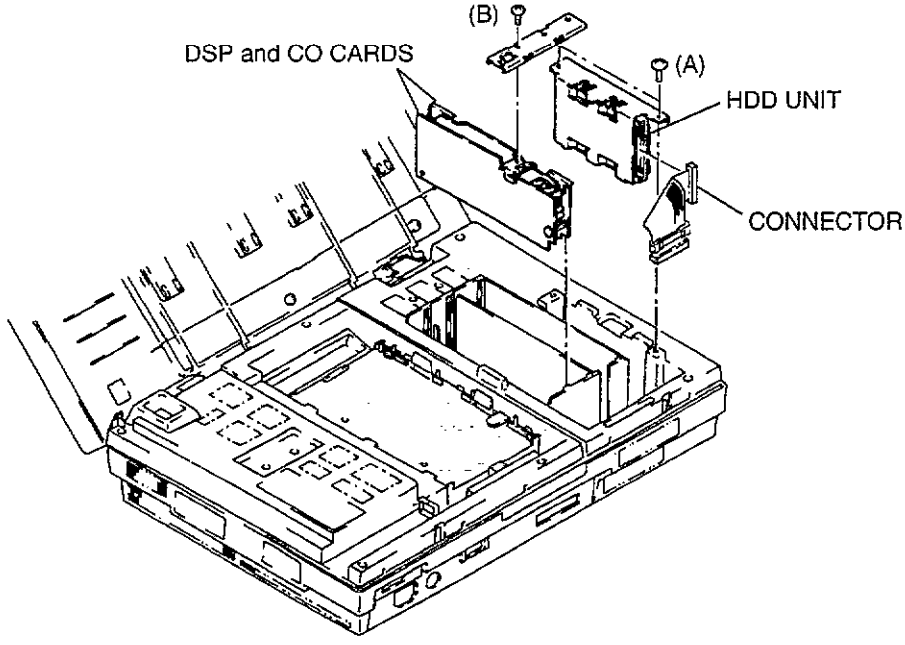
Ref. No. 1	HOW TO REMOVE THE FRONT COVER
Procedure 1	

1. Loosen the two screws (A).
2. Open the front cover.
3. Slide the front cover in the direction of the arrow when removing it.



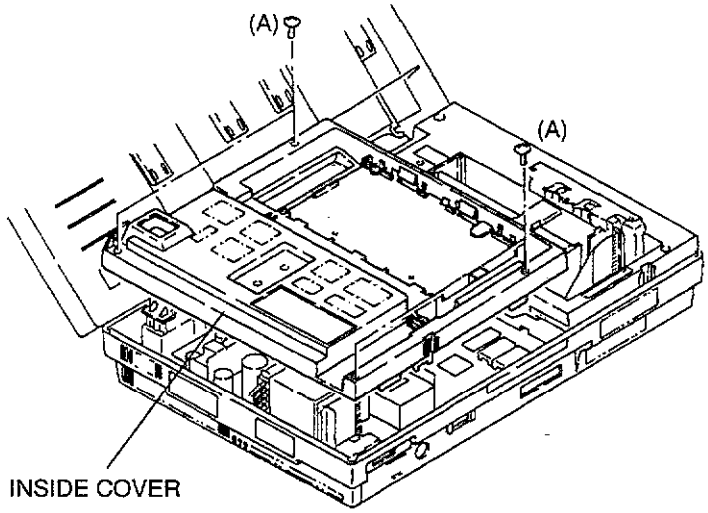
Ref. No. 2	HOW TO REMOVE THE HARD DISK DRIVE UNIT, DSP AND CO CARDS
Procedure 1 → 2	

1. Remove the two screws (A).
2. Pull out the connector from Hard Disk Drive Unit side.
3. Remove the Hard Disk Drive Unit.
4. Remove the screws (B).
5. Remove the DSP and CO cards.



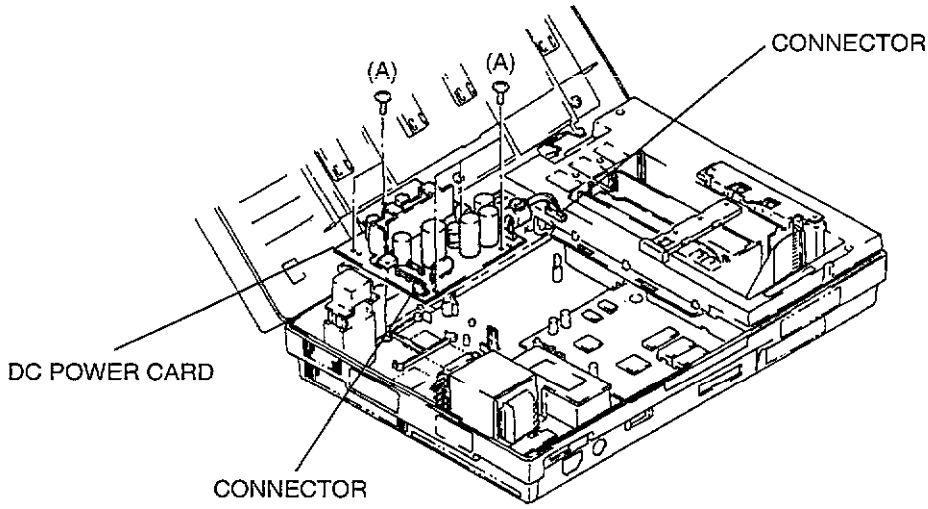
Ref. No.3	HOW TO REMOVE THE FRONT COVER
Procedure 1 → 3	

1. Remove the four screws (A).
2. Remove the Inside cover.



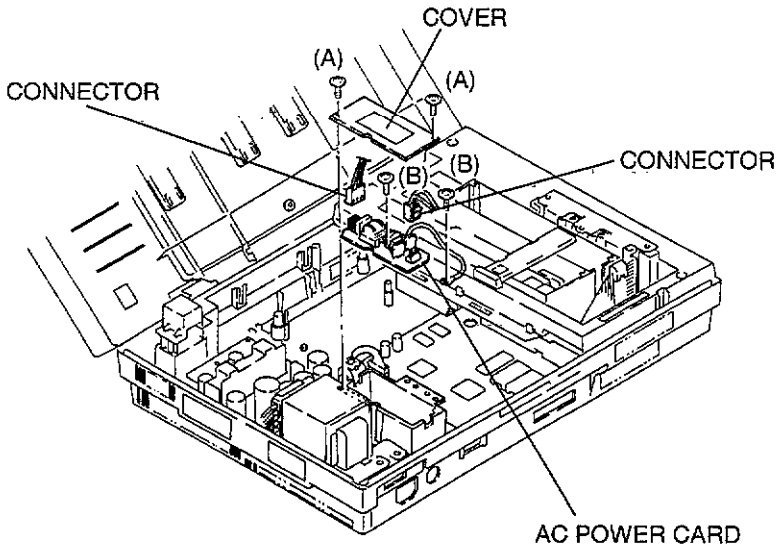
Ref. No. 4	HOW TO REMOVE THE DC POWER CARD
Procedure 1 → 3 → 4	

1. Remove the five screws (A).
2. Remove the two connectors.
3. Remove the DC Power Card.



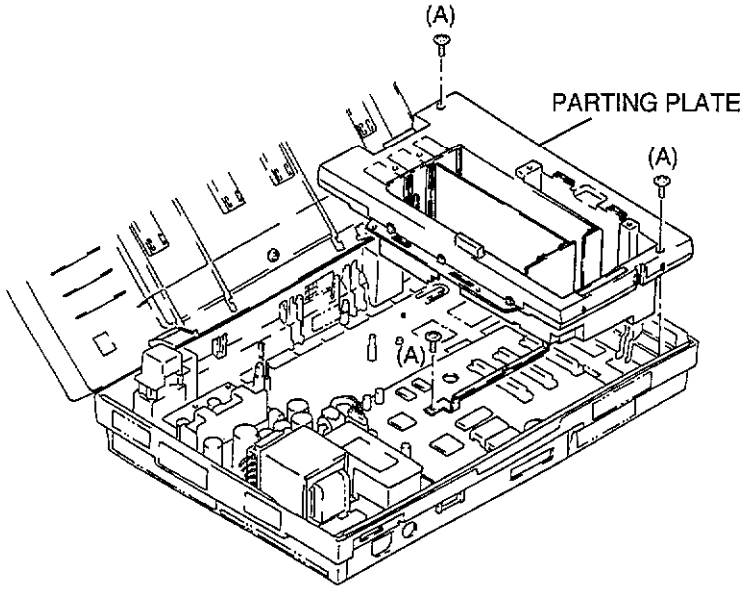
Ref. No. 5	HOW TO REMOVE THE AC POWER CARD
Procedure 1 → 3 → 5	

1. Remove the two screws (A).
2. Remove the cover.
3. Remove the two screws (B).
4. Pull out the two connectors.
5. Remove the AC Power Card.



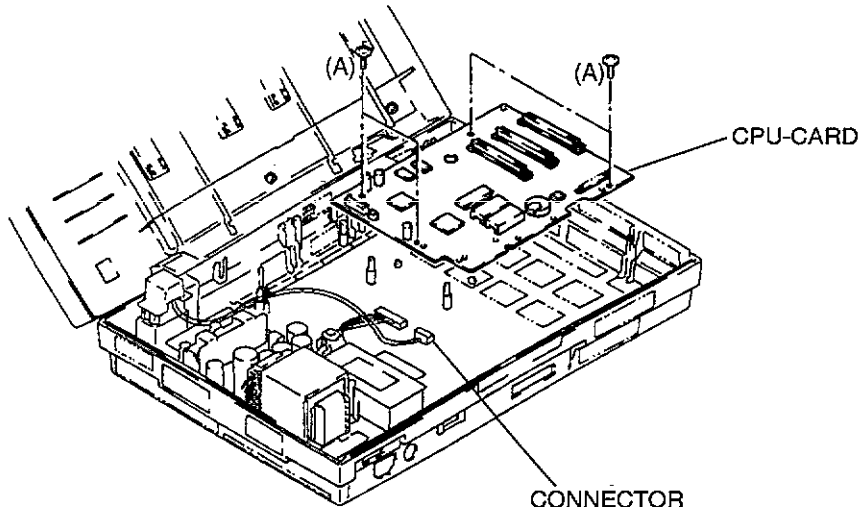
Ref. No. 6	HOW TO REMOVE THE PARTING PLATE
Procedure 1 → 2 → 3 → 6	

1. Remove the three screws (A).
2. Remove the Parting Plate.



Ref. No. 7	HOW TO REMOVE THE CPU CARD
Procedure 1 → 2 → 3 → 6 → 7	

1. Remove the four screws (A).
2. Pull out the connector.
3. Remove the CPU Card.



HOW TO REPLACE FLAT PACKAGE IC

■ PREPARATION

· SOLDER - - - - - - - Sparkle Solder 115A-1, 115B-1
OR
Almit Solder KR-19, KR-19RMA

· Soldering iron - - - - - Recommended power is 30 W to 40 W.
Temperature of Copper Rod 662 ± 50 °F (350 ±10 °C)

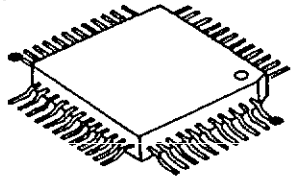
(An expert may handle 60~80 W iron, but a beginner might damage the foil by overheating.)

· Flux - - - - - - - - - - HI115 Specific gravity 0.863

(Original flux will be replaced daily.)

■PROCEDURE

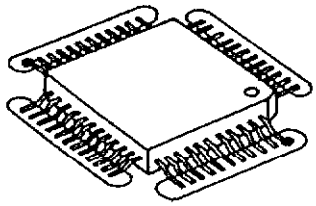
1. Temporarily fix the FLAT PACKAGE IC by soldering two marked pins.



●..... Temporary soldering point.

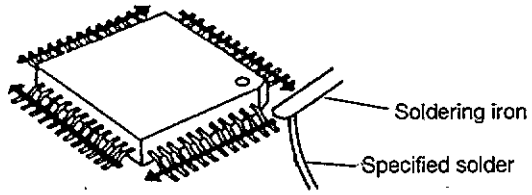
*Most important matter is accurate setting of IC to the corresponding soldering foil.

2. Apply flux to the all pins of the FLAT PACKAGE IC.



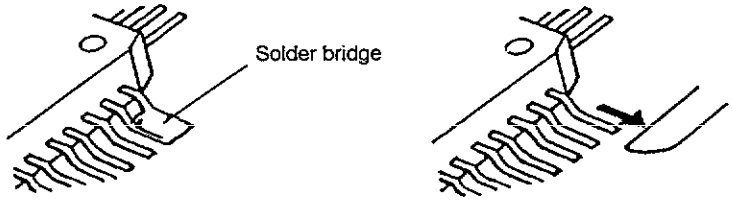
..... Flux

3. Solder the specified solder in the direction of the arrow, while sliding the soldering iron.



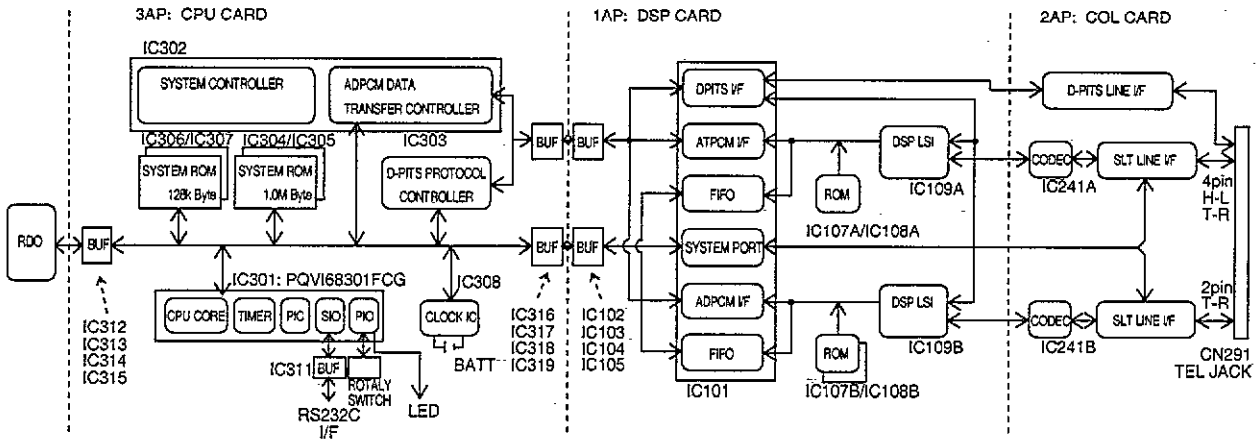
■MODIFICATION PROCEDURE OF SOLDER BRIDGE

1. Re-solder slightly on bridged portion.
2. Remove any remaining solder along the pins using a soldering iron as shown below.



FUNCTIONAL BLOCK DIAGRAM

VPS function block diagram is shown in Figure 3-1.



1. SYSTEM SPECIFICATIONS

The Table 3-1 shows the System Specifications.

Table 3-1. SYSTEM SPECIFICATIONS

ITEM	DESCRIPTIONS
Cabinet	Wall mounted type stand-alone style
Dimension (H × W × D)	468 × 327 × 101 mm (18-7/16" × 12-7/8" × 4")
Weight	7.0 kg
Power Source	AC 230-240 V, 50 Hz
Voice Storage Capacity	6 hours
Line Capacity Line connector Line interface	Basic 2 ports (maximum 4 ports) 4 pin moduler jack type connector Port-A: D-PITS/SLT Hybrid interface Port-B: SLT interface
Data Terminal Interface	Asynchronous RS-232C Port (25 pin Dsub connector) × 1 Data Rate: 300 up to 19,200BPS (programmable)
Operation Switches	Power Switch × 1 Mode Configuration Switch × 1 (only maintenance use)
LED	Power Indicator (red) × 1
Dialling Method	Tone duration/Pulse (10/20 pps)
Flash time	100/300/600/900 msec (programmable)
CPC detection	65/150/300/450/600 msec (programmable)
Extension numbering	2 to 5 digits (programmable)
Pause time	1 to 9 sec (programmable)
Message Waiting Lamp	Programmable DTMF sequence, or D-PITS data line
Number of Mailboxes	maximum 64
Number of Messages	100 per mailbox (programmable)
Personal Greeting Message Length	8 to 60 sec (programmable)
Message Retention Time	1 to 30 days, or unlimited (programmable)
Message Length	1 to 60 min (programmable)
Reports output	Mailbox list, Class of Service list, System Service report, Call Account report, Port Usage report, Mailbox Usage report, FAX report

2. CPU CARD

The CPU block is the main controller of the TVS100E. It adopts the micro processor (IC301 : PQVI68301FCG) of 68HC000 compatible. Its main CPU installs a Serial (RS-232C) Port, Parallel I/O Port, Timer, and Interrupt Controller.

Base Memory is ROM 128k byte (IC306/IC307) and RAM 1.0M byte (IC304/IC305). ROM stores the system initialize module, self diagnosis module, and system boot program from hard disk. RAM is used to execute system program and voice buffer to hold recording/compressed voice data for temporary play back.

The Main Board is loaded with a battery back up calender IC (IC308). It works as a time stamp function.

As an external interface, there is a hard disk interface (CN301) to control up to two units, non-same period RS-232C interface (CN307) by 19.2kBPS and three slot (CN301/CN303/CN304) of extension bus for I/O card connection with line interface module, etc.

The RS-232C interface is connected with Serial Port inside the IC301 through transceiver (IC311). As IC311 possesses a DC/DC converter, it generates +10V and -10V voltages needed for the RS-232C interface.

The extension bus is composed of an 8-bit parallel I/O bus and serial voice bus to transfer DMA data. Serial voice channel bus is an original bus in which serial data for two kinds/32 channels can pass through. ADPCM VOICE DATA (max 32kBPS) and D-PITS Data (max 32kBPS) are the data to pass through. DMA transfer with main memory is possible by Voice data combined with a DMA channel. D-PITS data is input and output from each line interface card to the HDLC controller (IC303) on the CPU Card.

In the VPS, this expansion slot is loaded with one line interface module in standard. One slot is released for increase of line interface module. The other one slot (Slot 3) is reserved for future application.

Table 3-2. SPECIFICATIONS OF THE CPU CARD

BLOCK	SPECIFICATIONS	DESCRIPTIONS
CPU	68EC000 compatible	Running frequency : 12.288 MHz (IC301)
RAM	1.0M byte	4Mbit Dynamic RAM × 2 (IC304/IC305)
ROM	128k byte	512Kbit IPROM × 2 (IC306/IC307)
INTERRUPT CONTROLLER	10 levels	hardware interrupt request notify to CPU (IC301)
TIMER	3 Channels	for using the system management (IC301)
RS-232C I/F	1 Channels	Asynchronous (300 - 19.2kBPS) (IC301)
Pararell I/O Port	13 bits	for using LED on/off, Rotary Switch sensing (IC301)
D-PITS I/F	CCITT X.25 Level-2	D-PITS Protocol Control (IC303)
System Controller	Custom LSI	for the all of the system timing control (IC302)
CLOCK	Real Time Clock	with Battery Backup (IC308)
HDD I/F	44pin connector × 1	connecting upto 2 Hard Disk Drives (IC301)
EXP. SLOT	50pin connector × 3	connecting DSP/COL module (IC302 to CN304)

3. DSP CARD

DSP block is loaded with DSP (IC109) installed with a 1.3k word RAM and 32k word outside the fixed program ROM (IC107/IC108).

This DSP interfaces CODEC, connected with a SLT interface on a COL block and transforms voice region signals D/A, A/D, and D-PITS line.

Each DSP disposes a digital voice region data for each channel described below. Mutual transformation, voice region digital data (64kBPS : 8bit/125us) and ADPCM data (32kBPS : 4 bit/125us), are executed. To detect a certain tone (for example DTMF tone or call progress tone) by analyzing input PCM data and to output a certain tone (for example DTMF tone or BEEP tone) as PCM data.

Timing Control on the DSP block is controlled by the system controller (IC101). System controller includes D-PITS interface, ADPCM compressed voice data transfer control between DSP and system memory, FIFO logic and parallel I/O port to control the SLT circuit line.

DSP receives commands from the host CPU through FIFO (IC101), then works based on the command.

This DSP execution program is stored in the external high speed ROM (IC107/IC108).

The D-PITS interface logic works to input and output the information data (D channel data) received and sent with the PBX through D-PITS with a HDLC controller (IC303) on a CPU block. It distributes voice region data (B1,B2 channel data) received and sent by the PBX through a D-PITS to each DSP(IC109A, IC109B).

The Parallel I/O port, used for SLT interface on the COL block taking status and Hook control, is controlled by the CPU.

4. COL CARD

A port in the COL block is a hybrid component and is constructed to add an SLT interface with loop start style to the D-PITS transceiver.

It is intended to detect the arrival of signals (BELL), to catch circuits (DC loop enable), and to generate a dial pulse by loop on/off and 2-line ~ 4-line transformation (Balance-Network) as a basic function. The 4-line analog data is transformed to digital data by CODEC, then is interfaced with the DSP block.

The D-PITS transceiver includes the transceiver by transistor (Q261/Q262) and receiver by converter (IC261) and interfaces with PBX through the Pulse Trans (T291).

Table 3-3. SPECIFICATIONS OF THE DSP CARD

BLOCK	SPECIFICATIONS	DESCRIPTIONS
HOST I/F	50-pin Connector	Signals ×38, +5V ×2, -5V ×2, GND ×8
COL I/F	30-pin Connector	
DSP LSI (IC109)	Internal RAM	Running frequency : 57.344MHz (14.336MIPS)
	Internal ROM	1312 word ×16 (for Program/Data memory)
	Serial Port	20kword ×16 (not used)
	CODEC I/F	using D-PITS digital voice data in/out
		using SLT analog voice data in/out
DSP ROM (IC107/IC108)	64kByte (IC107/IC108)	access time : 35 nsec
SLAVE CONTROLLER (IC101)	FIFO	To communicate between Host CPU and DSP
	Parallel I/O Port	bit IA-3 : not used
		IA-2 : CPU-A detect when 0
		IA-1 : not used
		IA-0 : BELL-A detect when 0
		OA-1 : not used
		OA-0 : HOOK-A control (0: off-hook)
		IB-3 : not used
		IB-2 : CPU-B detect when 0
		IB-1 : not used
		IB-0 : BELL-B detect when 0
		OB-1 : not used
		OB-0 : HOOK-B control (0: off-hook)
		OX-3 : not used
		OX-2 : not used
		OX-1 : loop test enable when 0
		OX-0 : not used
	Serial Voice Port	for ADPCM Voice Data Transfer Control between DSP and System Memory
	D-PITS interface	D-PITS Frame Formatter and Transceiver

Table 3-4. SPECIFICATIONS OF THE COL CARD

<table>
<tr><th>BLOCK</th><th>SPECIFICATIONS</th><th>DESCRIPTIONS</th></tr>
<tr><td>DSP I/F</td><td>30 pin Connector</td><td></td></tr>
<tr><td>COL I/F</td><td>4 pin Moduler × 2</td><td>Port-A : D-PITS/SLT Hybrid I/F
Port-B : SLT I/F</td></tr>
<tr><td rowspan="3">T-R I/F</td><td>BELL Detect</td><td>To Detect the following Bell Signal
Voltage : min 40 Vrms (Frequency : 25 Hz)
The H/W only detects the level/frequency.
The bell cadence should be checked by software algorithm.</td></tr>
<tr><td>DIAL PULSE Control</td><td>The hardware logic only controls the loop ON/OFF.
Pulse Dialling Cadence is controlled by S/W
Dialing Rate: 10 or 20 PPS
Break to Make Ratio : 60 %
Interdigit Interval : Typical 800 ms</td></tr>
<tr><td>DTMF TONE Dialling</td><td>DTMF tone is generated by DSP LSI, and DSP sends the DTMF tone to CODEC or D-PITS.
-Tone Level : High Group : -9 dbm
Low Group : -11 dbm
Twist 2 dbm
Harmonics Level: -7 dbm
-Digit Layout : Refer to following Table
High Group [Hz]
<table><tr><th></th><th></th><th>1209</th><th>1336</th><th>1477</th><th>1633</th></tr><tr><td>Low Group</td><td>697</td><td>1</td><td>2</td><td>3</td><td>A</td></tr><tr><td>[Hz]</td><td>770</td><td>4</td><td>5</td><td>6</td><td>B</td></tr><tr><td></td><td>852</td><td>7</td><td>8</td><td>9</td><td>C</td></tr><tr><td></td><td>941</td><td>*</td><td>0</td><td>#</td><td>D</td></tr></table>
-Frequency Tolerance : max +/- 1.5%
-Duration : 80 msec
-Interdigit Interval : 100 msec</td></tr>
</table>

5. HARD DISK DRIVE

VPS uses a 2.5" intelligent magnetic disk device as an accumulator of voice data and storage of system program.

Table 3-5. SPECIFICATIONS OF THE HARD DISK DRIVE

	MK1722FCV
Format capacity (MB)	131
Actuator type	Rotary voice coil motor
Servo form	Data face sector servo
Format formular	Hard Sector
Disk	1
Data head	2
Cylinder for user	1,920
Format track capacity (B)	28,672
Sector length (B)	512
All sectors for user	168,112
Sectors per track	
Physical sectors	57
Sectors for user	56
Recording form	1-7RLL
Track density (track/mm)	139
Maximum line recording density	
(bit/mm)	2,690
(flux change/mm)	2,010
Access time (ms)	
Neighboring track	3
Average	13
Maximum	25
Average rotation waiting time (ms)	7.5
Rotation (rpm)	4,000
Rotary precise degree (%)	±1.0
Data transfer speed	
Host transfer (MB/S)	11.1
Disk transfer (Mbps)	18.9~31.6
Sector interleave	1 : 1
Tracks queue	Exists
Buffer size (KB)	128
Cache	Read Ahead Cache
Starting time (s)	
(till drive ready)	4 (Average), 20 (Maximum)
Stopping time (s)	
(when power source cut off)	7 (Average), 10 (Maximum)
Stand-by recovering time (s)	4 (Average)

6. POWER SUPPLY

Power Source Unit generates two kinds DC voltages (+5 V/-5 V), then supplies to the system.
Inside the main power supply, there is a voltage maintain circuit with big capacitor. That's why DC voltage is supplied steadly, in spite of AC voltage going lower temporary. The maximum DC voltage supply period by this capacitor is 700msec.
This Power source asserts DC alarm signal, when +5V DC voltage goes lower than a certain threshold level. This signal is connected to Parallel Port inside IC301 through connector, Microprocessor can always check falling DC voltage. Power save disposition is executed when DC alarm signal assertion from power source is detected.

Table 3-5. SPECIFICATIONS OF THE POWER SUPPLY

BLOCK	SPECIFICATION	DESCRIPTION
+5V	DC-DC Converter	Output Voltage 5V The maximum output current 3A Momentary output current 3.5 A Efficiency 75% TYP Input voltage range 8V ~ 32V Switching frequency 70khz Over current protection More than regulated current, voltage goes down, Recover automatically Over Current protection exists
-5V	Regulator	Output Voltage -5V Output Current 1A The minimum difference of input and output 2V Over Heat Protection exists ASO Protection exists
Over Voltage Detection		More than 5.7V, +5V output is cut off.
DC Alarm		Less than 4.7V, alarm signal is issued.

CIRCUIT OPERATION

1. CPU CARD

1-1. System Reset (IC310)

When the power is on, the System Reset IC (IC310) initializes the whole system. MRSTN, output from IC310, is input to the RSIN (119 pin) of IC302. During RSIN's low period, IC302 is self-initialized and drives LRSTN (49 pin) and HLTN (50 pin) to low order to make the external device initialize.

LRSTN is distributed as shown below. LRSTN should be driven in High level normally. Only when the power is on, it is asserted in Low.

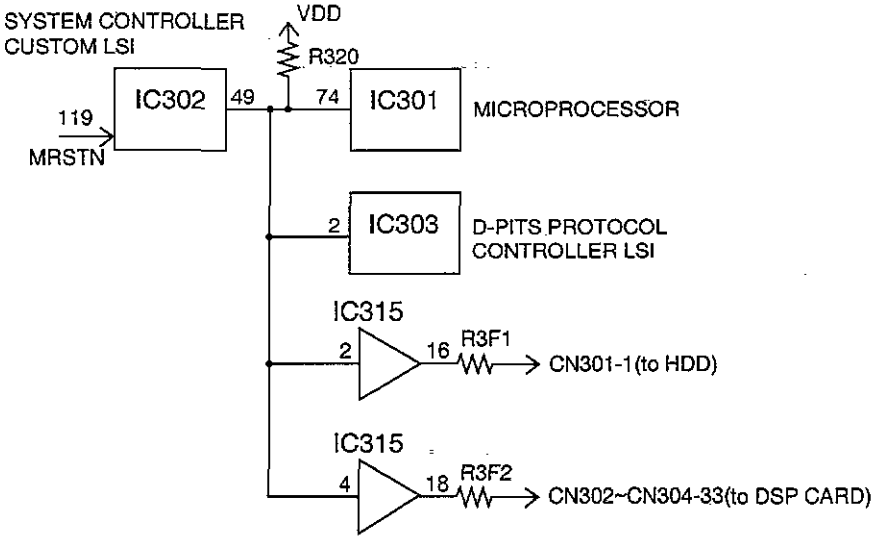
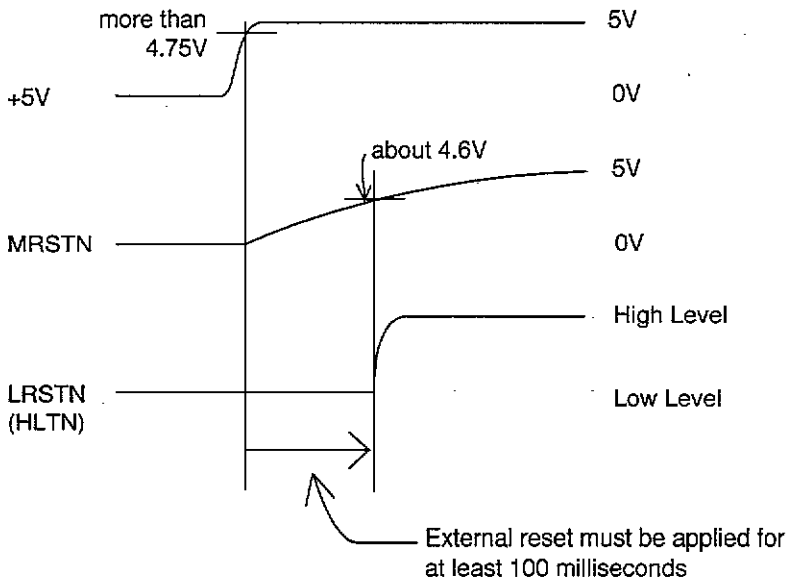


Fig. 4-2. System Reset Distribution



Timing 4-1. System Reset

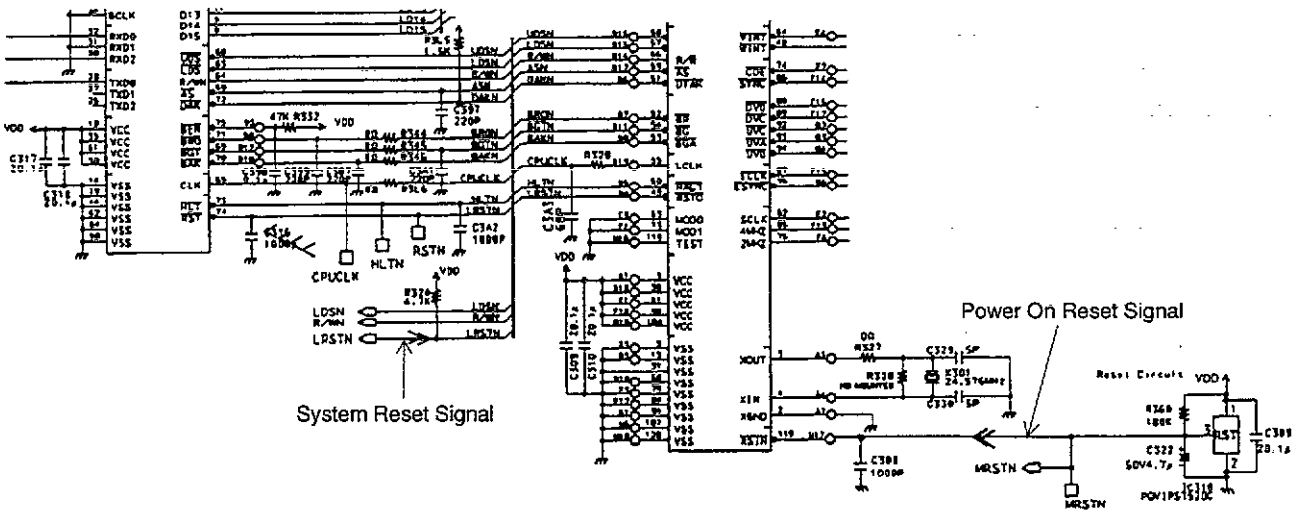


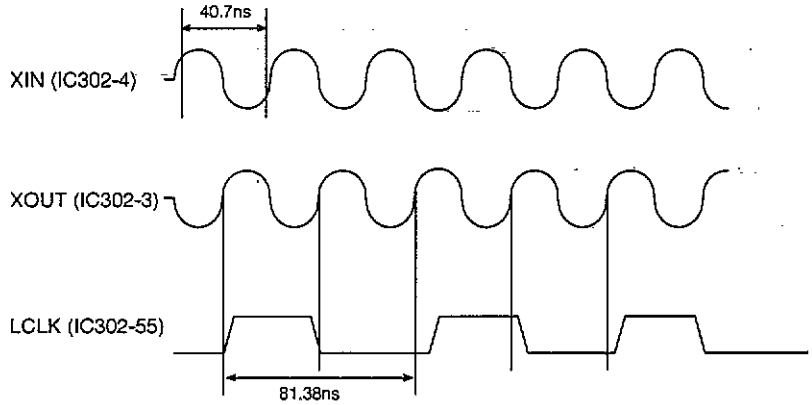
Fig. 4-1. System Reset Signal Flow

1-2. Microprocessor Interface (IC301, IC302)

System controller (IC302) controls the Microprocessor (IC301) to access external resources (i.e. Memory, I/O device).

(1) Processor Clock

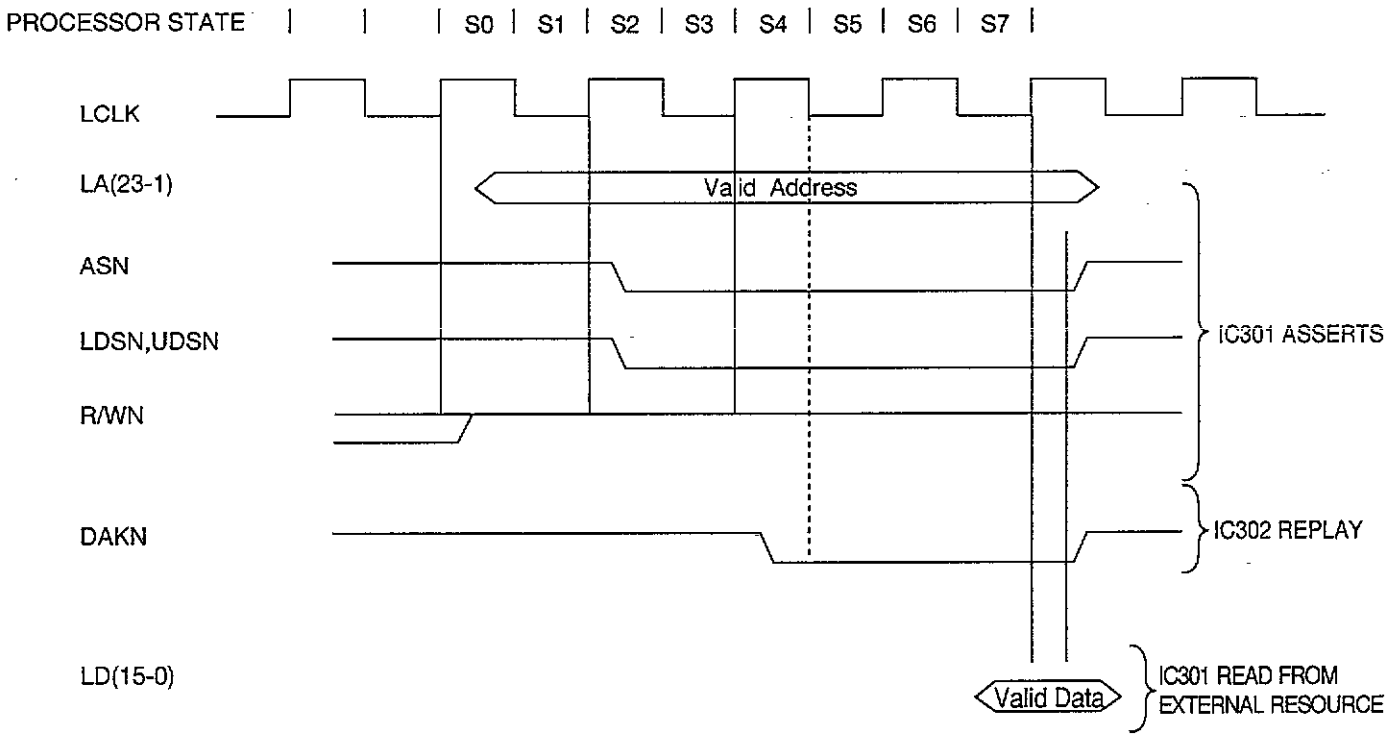
IC302 provides a processor clock from the LCLK (55) pin. Output of X'tal connected to IC302 is output from the LCLK pin divided in half inside the IC302.



Timing 4-2. Processor Clock

(2) Read Cycle

In the read cycle IC301 outputs a valid address to A(23-1) in S0 state. Then in S2 state, IC301 asserts a signal line of ASN(59), UDSN(60), LDSN(63) and R/WM(64). IC302 decodes the condition of these signal lines and replies to DAKN(IC302-5 pin) in needed timing (normally in S4 state). By DAKN's reply, IC301 reads the valid data on the LD(15-0) line. (refer to Timing 4-2).



Timing 4-3. Read Cycle

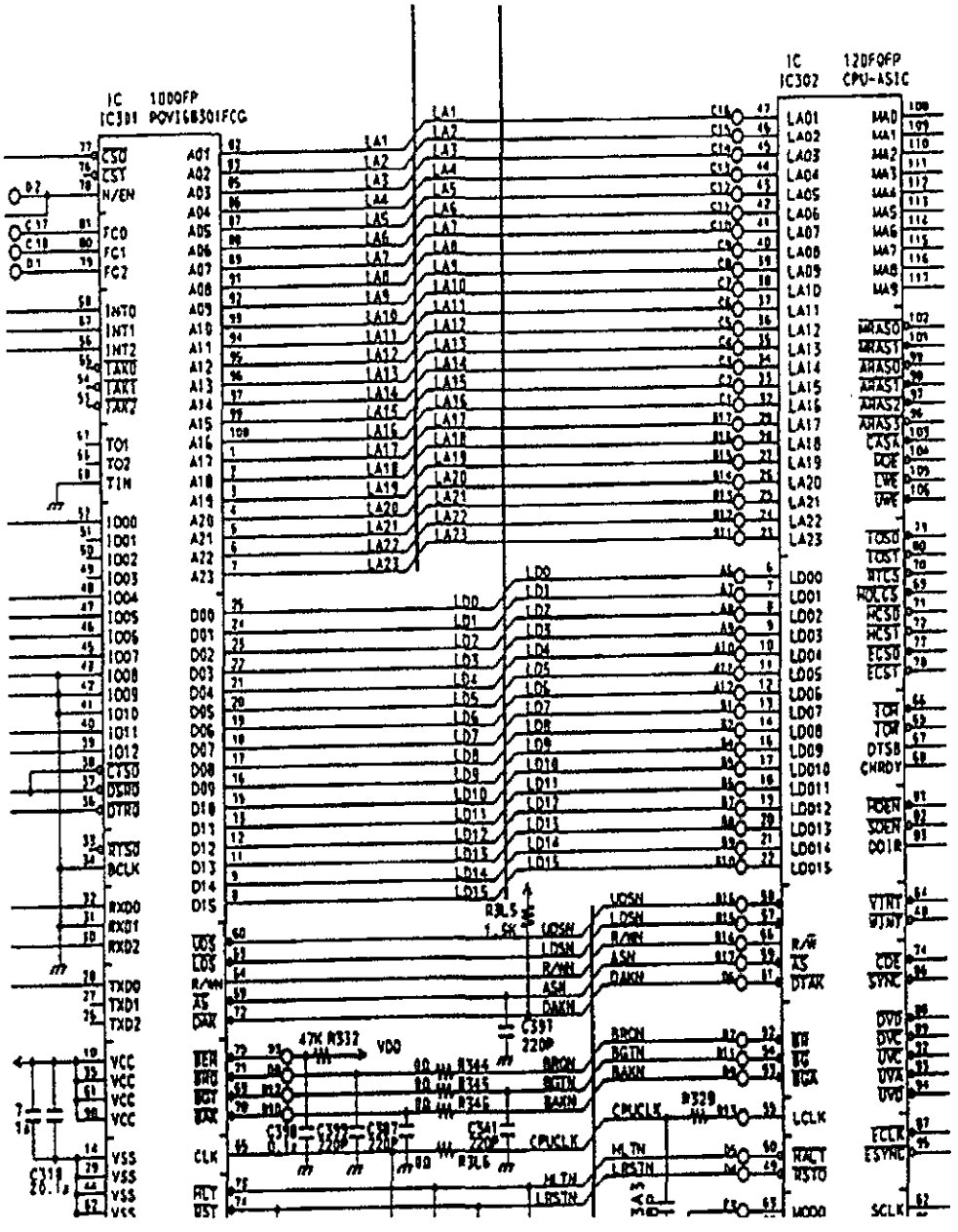
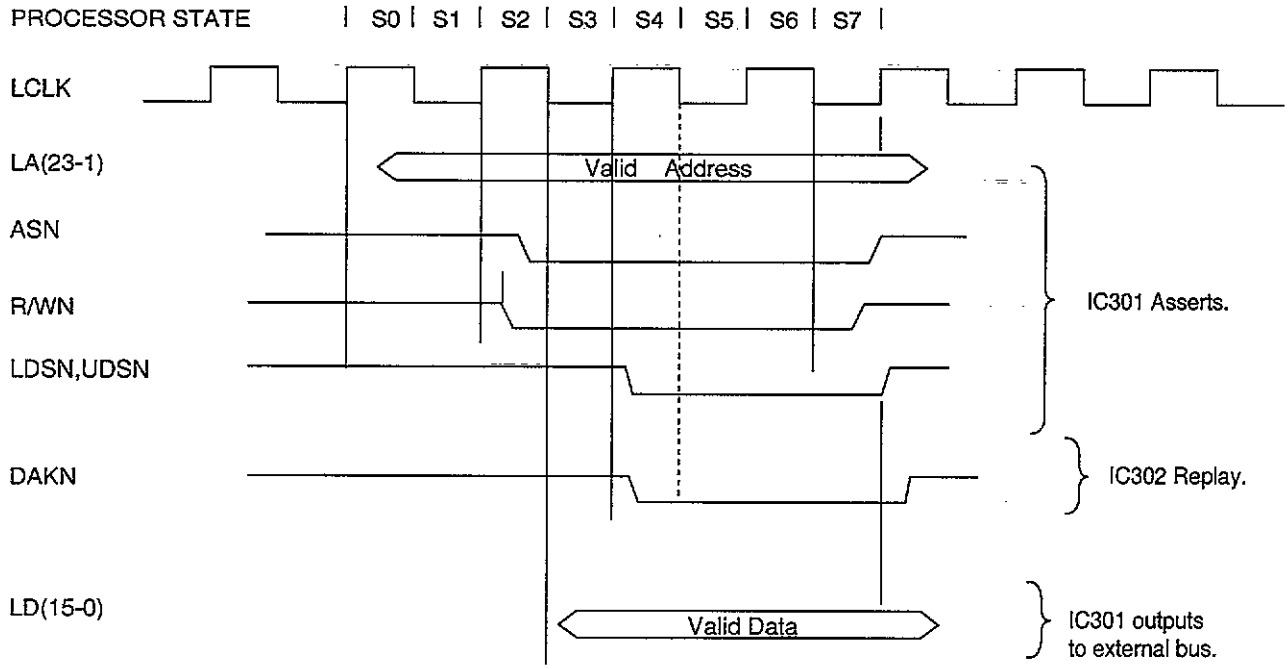


Fig. 4-3. Microprocessor Interface

(3) Write Cycle

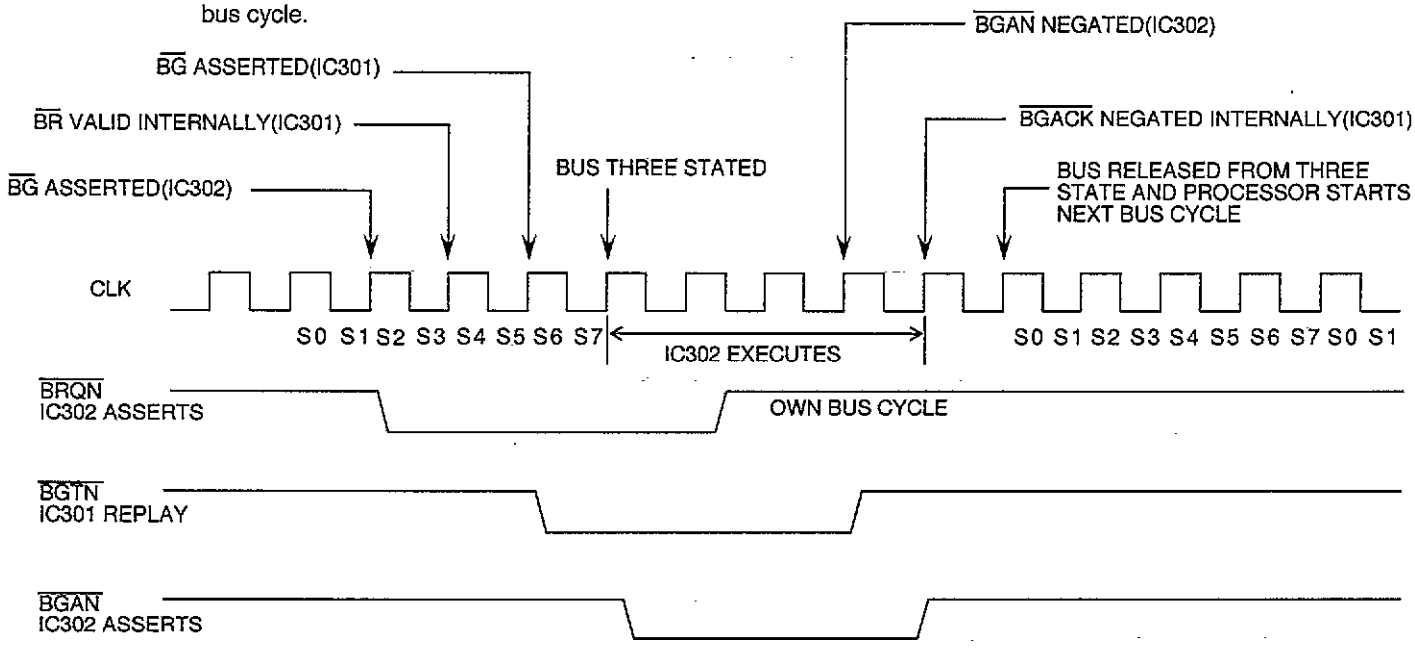
In write cycle IC301 outputs valid address to A(23-1) in S0 state. Then in S2 state, IC301 asserts a signal line ASN(59), R/WN(64). In S3 state, it outputs valid data to LD (15-0). In S4 state it asserts the signal line of UDSN(60) and LDSN (63). IC302 decodes the condition of these signal lines and replies to DAKN(IC302 - 51pin) in needed timing (normally in S4 state). IC302 terminates write cycle by the reply of DAKN. An External resource is controlled to take in effective data on LD(15-0) by a control signal generated from the system controller.



Timing 4-4. Write Cycle

(4) Bus Arbitration Cycle

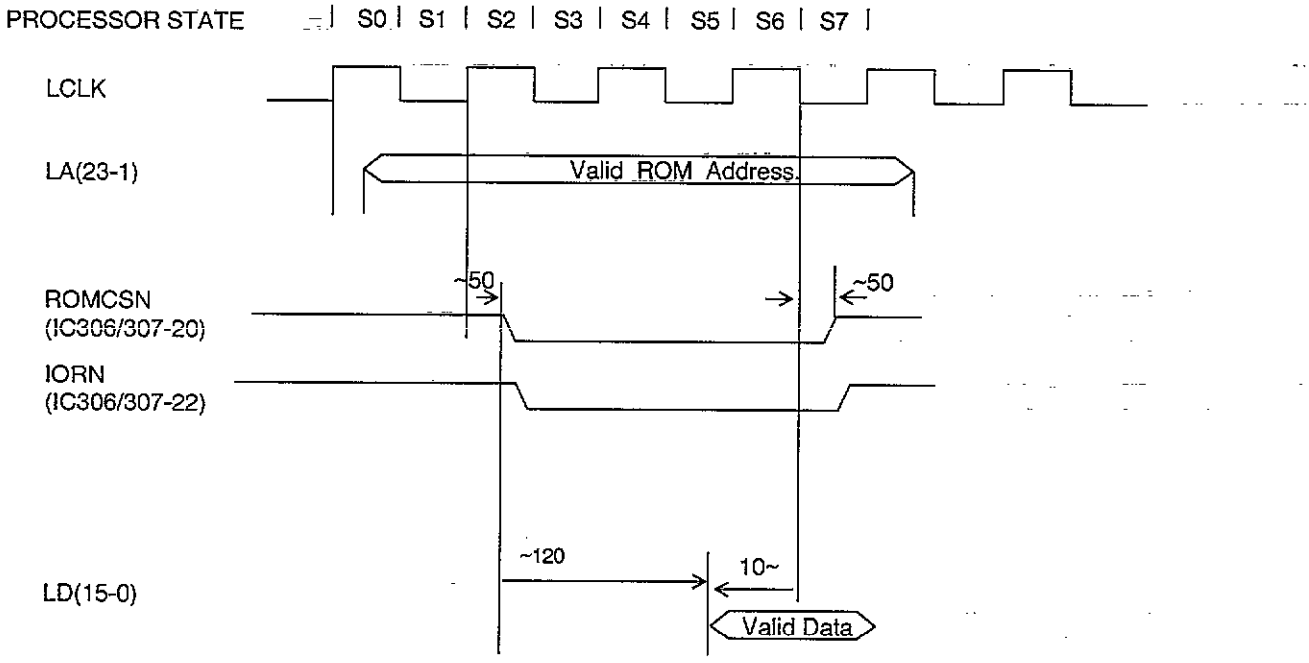
The system controller (IC302) itself should access to system memory (i.e. transfer to system memory of ADPCM Data, execution of DRAM refresh). System controller (IC302) requires the Microprocessor (IC301) to hand over bus ownership with asserting BRQN (IC302-52 pin). When IC301 finishes its own bus cycle, it replies to BGTN(IC301 - 69) and hands over bus ownership to IC302. After detecting assertion of BGTN, IC302 asserts BAKN (IC302 - 53) then executes access to system memory for itself. At that time IC302 negates BRQN. After terminating the access to system memory, IC302 negates BGAN to hand over Bus ownership to the Microprocessor (IC301). After detecting negation of BGAM, IC301 starts executing its own bus cycle.



Timing 4-5. Bus Arbitration

1-3. System ROM (IC306, IC307)

System ROM has a program to initialize the system, diagnose itself and a loading program to load the application program from HDD to System RAM. Right after System Reset is negated, the Microprocessor (IC301) always reads the program execution address stored in the address "00000h" of System ROM. Based on that execution address information, IC301 starts to execute program initializing Inside the system of ROM.



Timing 4-6. System ROM Read

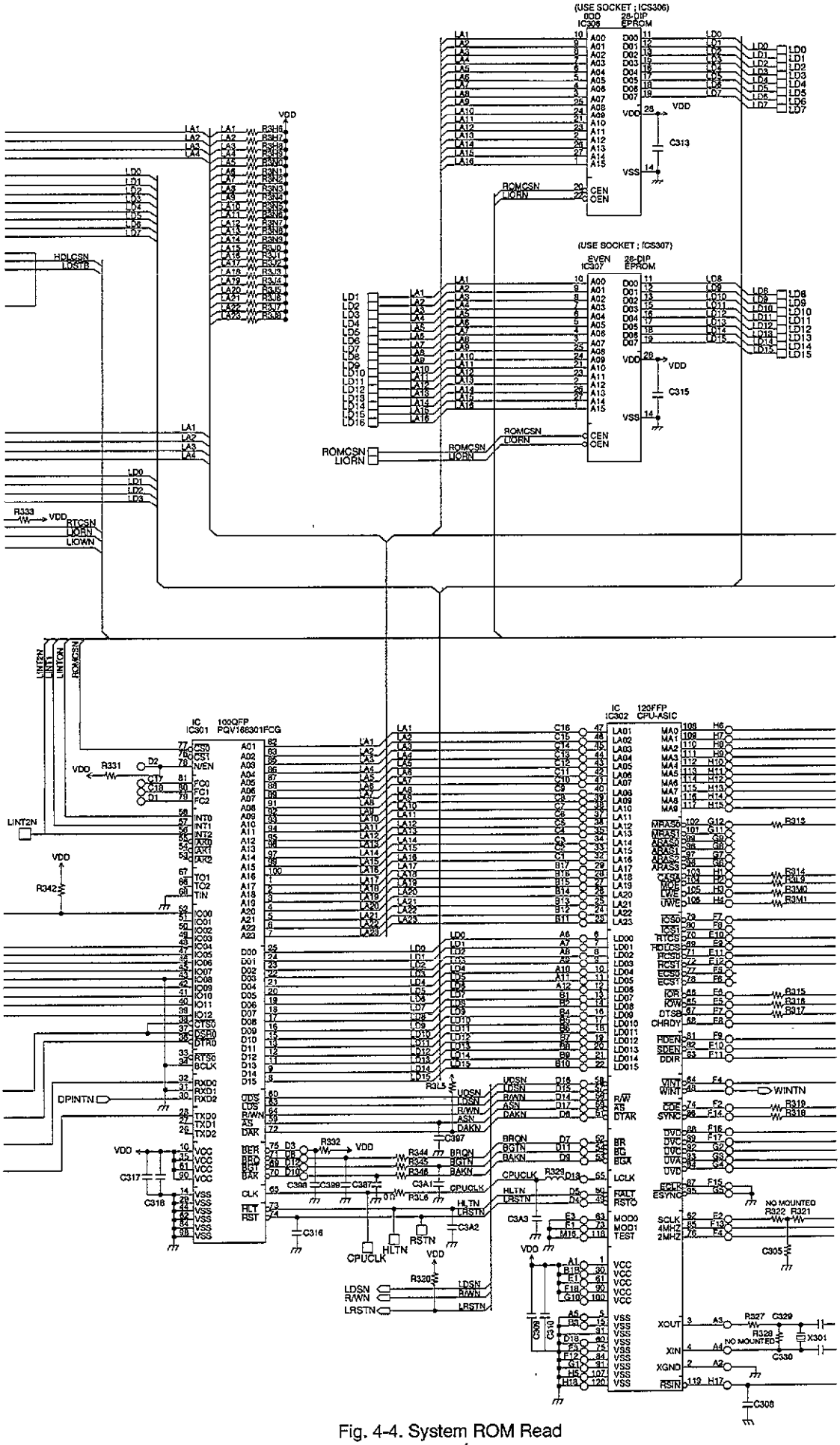


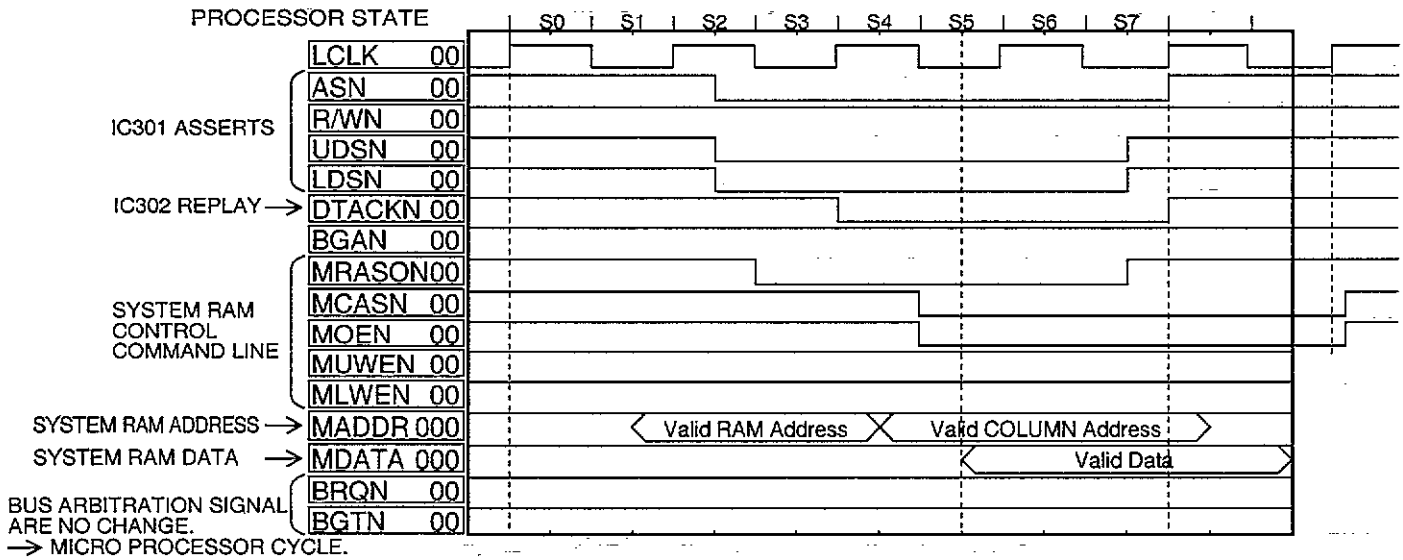
Fig. 4-4. System ROM Read

1-4. System RAM (IC304, 305)

An Application program is loaded to system RAM by a ROM based Program. The execution program will then run on the system RAM. System RAM uses a 4M bit Dynamic RAM . This access timing is controlled by the system controller (IC302).

(1) System RAM Read Cycle. by Microprocessor

Microprocessor executes a normal read cycle in the system RAM's Read cycle by a IC301 (Microprocessor). IC302 (System controller) decodes the condition, then generates the dynamic RAM's read signal.



Timing 4-7. System RAM Read Cycle by Microprocessor

In read cycle MRASON(IC302 - 102, memory RAM address strobe) is asserted in low in the falling edge of the S2 state. IC303 and IC304 take address information on MA(9-0) in MRASON falling edge. Next MA(9-0) changes in S4 state. CASN(IC302 - 103) (Column Address Strobe) and MOEN (IC302-104) (Memory Output Enable) are asserted in low in S4 stat's falling edge. IC303 and IC304 take address information on MA(9-0) in CASN's falling edge. They output their own data to LD(15-0) because MOEN is asserted.
The Microprocessor takes effective data on LD(15-0) in S6 state falling edge.

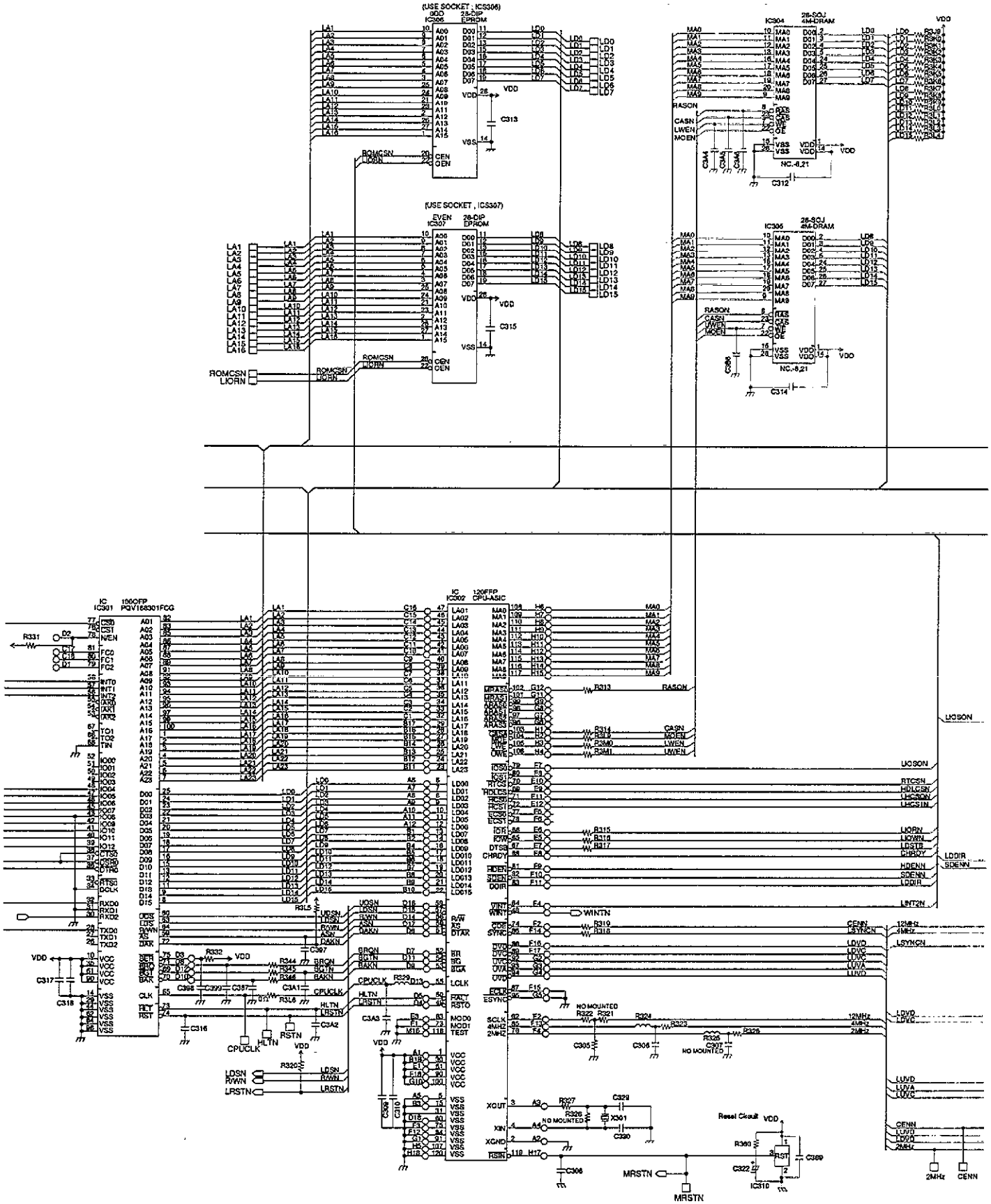
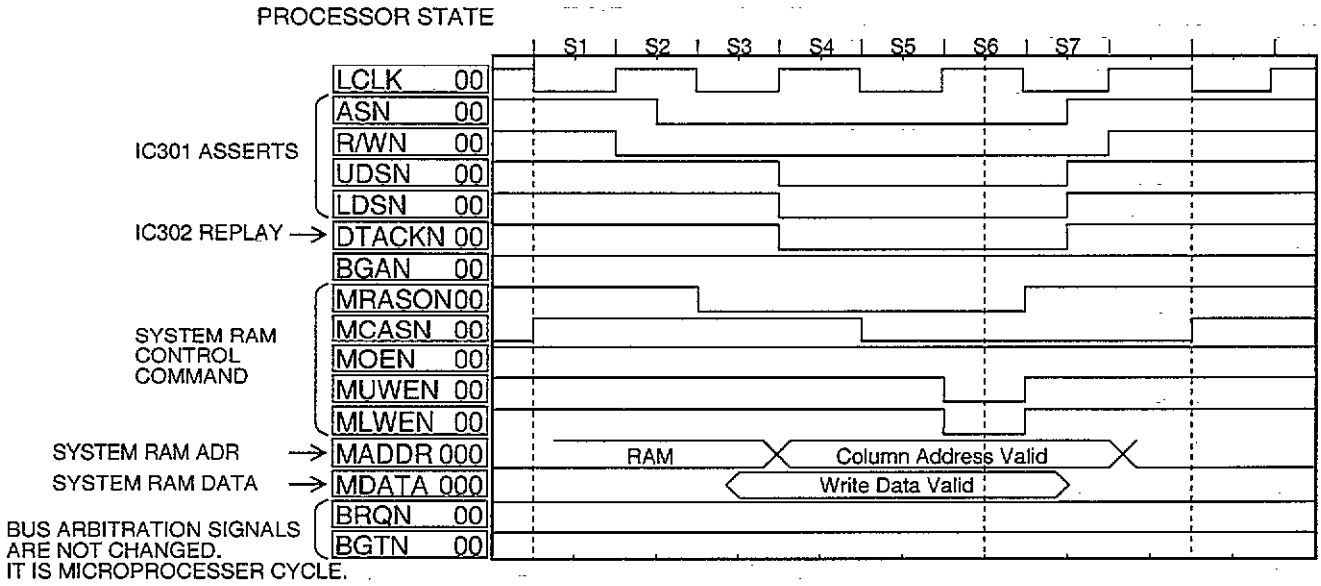


Fig. 4-5. System RAM

(2) System RAM Write Cycle by Microprocessor



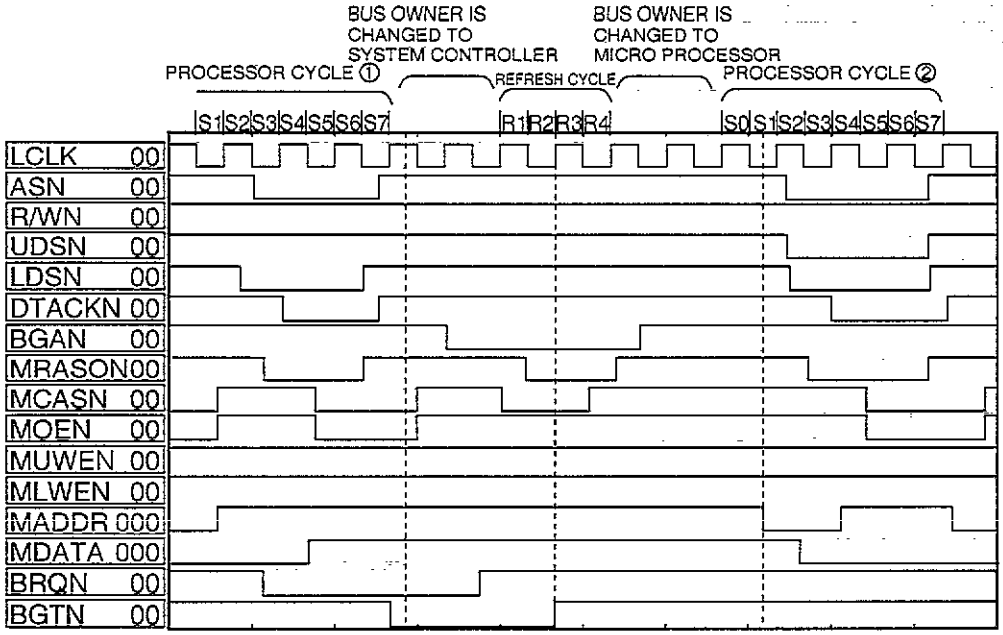
Timing 4-8. System RAM Write Cycle by Microprocessor

In System RAM Write Cycle by Microprocessor, MRASON (IC302-102) = Memory RAM Address Strobe, is asserted in low in the falling edge of the S2 state. IC303 and IC304 take address information on MA(9 - 0) in the falling edge of MARASON. MA(9 - 0) varies in S4 state. CASN (Column Address Strobe) is asserted in the falling edge of S4 state. IC303 and IC304 take address information on MA(9 - 0) in the falling edge of CASN. IC301 outputs the effective data to LD(15 - 0), the period from S3 state to S6 state. IC302 asserts UWEN (106) = Upper memory write enable and LWEN (105) = Lower Memory Write Enable, in S6 state. IC303 and IC304 take the data on LD(15-0) in the falling edge of UWEN and LWEN into the inside of memory.

(3) Refresh Cycle by System Controller

In order to preserve the internal data of the Dynamic RAM used as System Memory, System Controller (IC302) executes a bus cycle, called Refresh cycle, every 16μs. In order to execute the Refresh Cycle, System Controller demands Bus Ownership from Microprocessor (IC301) . After receiving bus ownership from the Microprocessor, System Controller executes Refresh cycle. After the Refresh cycle is completed, System Controller hands over Bus Owner ship to the Microprocessor. (Refer to 1-2. (4) Bus Arbitration Cycle). The Refresh cycle executed is called "CAS BEFORE RAS Refresh". In case of not being executed periodically, the Refresh cycle is hold in the Dynamic RAM. The Data is purged.

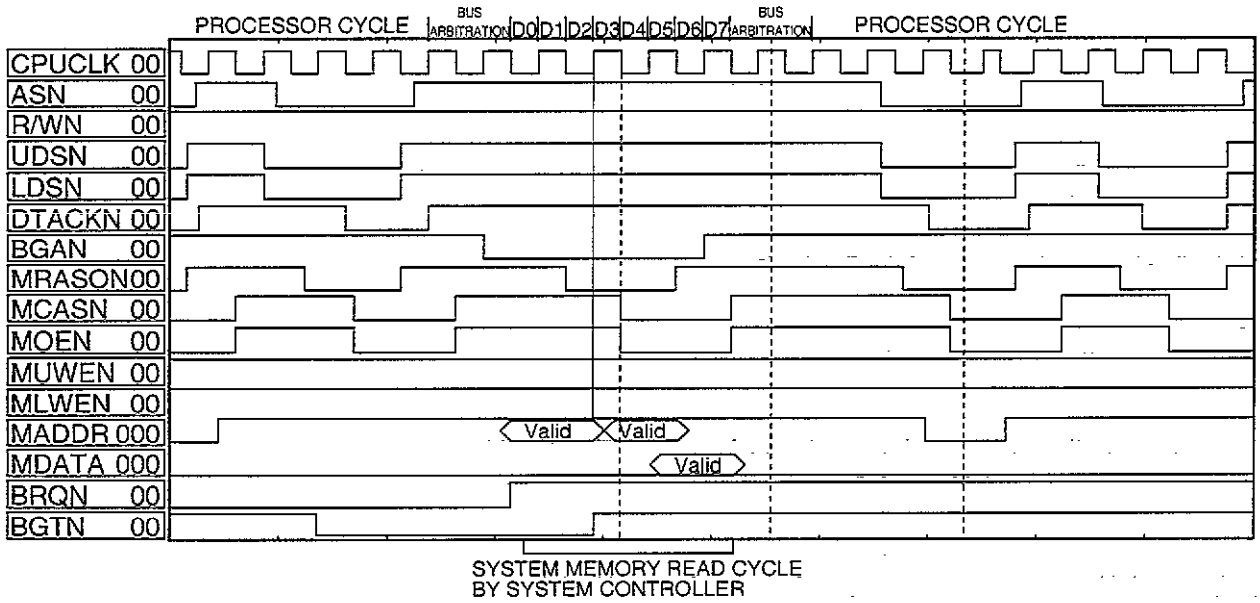
The Refresh cycle is executed while BGAN (IC302 - 53) is asserted, namely system controller is in the period of Bus Ownership. This cycle starts from LCLK (IC302 - 55)' s rising edge after the BGAN is asserted, then is completed during 2xLCLK. CASN (IC302 - 103) is asserted in the rising edge of R1 state. Each of them is negated in the falling edge of R3 state and in the rising edge of R4 state. Around Refresh Cycle Arbitration cycle is executed.



Timing 4-9. Refresh Cycle by System Controller

(4) System RAM Read Cycle by System Controller

In time Message Delivery to the extension line, the DSP Card requires System Controller (IC302) to send the ADPCM Data on System memory. System controller, accepting this requirement, demands Bus Ownership from the Microprocessor (IC301). Once System controller receives Bus Ownership from the Microprocessor, the System RAM read cycle is executed. After that System Controller hands over Bus Ownership to the Microprocessor.



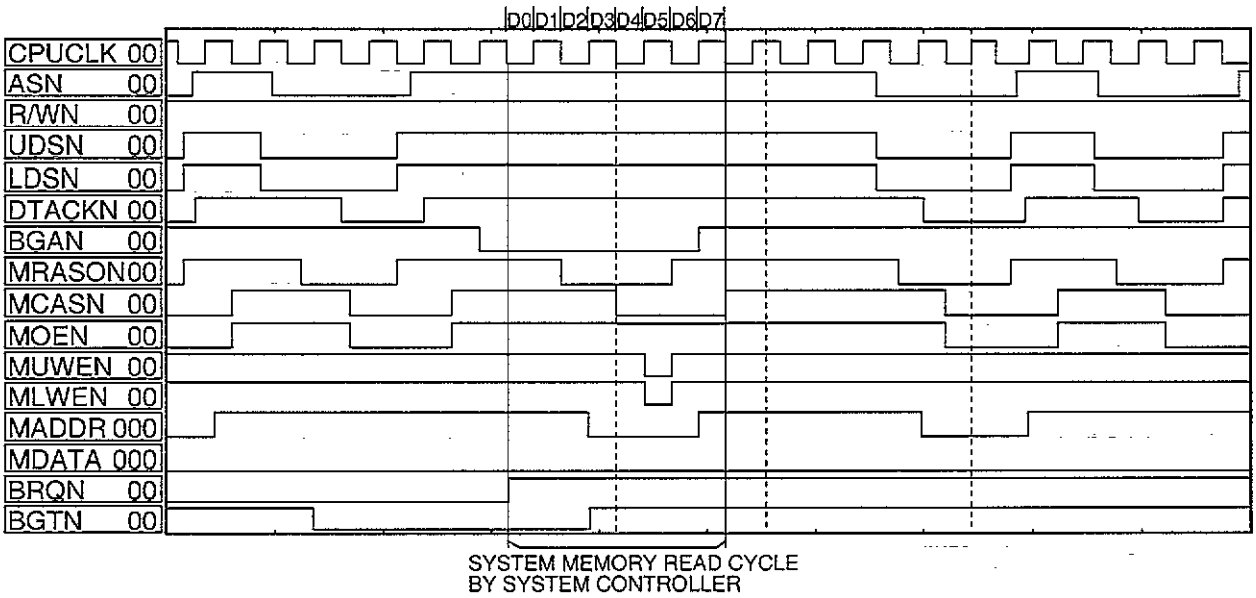
Timing 4-10. System RAM Read Cycle by System Controller

Once System Controller rewires Bus Ownership from the Microprocessor, it asserts BGAN (IC302 - 53) in low and executes the System - Memory Read cycle. This read cycle starts from CPUCLK's rising/falling edge after BGAN is asserted and ends during 4xCPUCLK.

The System Controller outputs a destination address to MA(9 - 0) in D0 state. MRASON is asserted in the leading edge of D2 state and MA (9 - 0) switches over in D3 state of the leading edge. MCASN and MOEN are asserted in the leading edge of D4 state. IC303 and IC304 start outputting the data to LD (15 - 0). System controller takes in the effective data on LD(15-0) in the leading edge of D7 state. (The data taken in is sent to the DSP Card through the extension bus. In order to return bus ownership to the Microprocessor, System controller negates BGAN in the leading edge of D7 state.

(5) System RAM Write Cycle by System Controller

In time Message receiving from the extension line, ADPCM data generated by the DSP is added to the system RAM address information of where to transfer the DSP card. Then ADPCM data is sent to the system controller. Receiving this information, System Controller requires the Microprocessor to hand over Bus ownership in order to write designated addresses. By this requirement, system controller obtained bus ownership executed by the System Ram Write cycle.



Timing. 4-11 System RAM Write Cycle by System Controller

In Write cycle by System Controller, the output timing of MRASON, MA(9 - 0) and MCASN are the same as the Read cycle. In Write cycle MOEN is not asserted , and MUWEN and MLWEN are asserted in D5 state. In time, BGAN is asserted in low, System Controller outputs effective data to LD (5 - 0). This effective data is stored in IC303 and IC304 at the falling edge of MUWEN and MLWEN .

1-5. System Port

The System Port Function is provided by PIO (Parallel Input Output Control) inside IC301.
System Port's functions are

- to control the Power Indicator (LED)'s ON/OFF
- to read the condition of the Rotary switch
- to read the condition of DCARM (DC Alarm) input from the Power Unit.

(1) Power Indicator (LED) ON/OFF control

The Power Indicator (LED)'s ON/OFF is controlled by a IC301 - pin 51. This pin is connected to the base of the digital transistor Q301. When IC301 - 51 is "High", between the emitter and collector of Q301, it becomes transmissible and LED turns on. When IC301 - 51 is "Low", between emitter and collector of Q301, it becomes non-transmissible and LED turns off.

(2) Rotary switch port

The Rotary switch is surrounded by IC301 - pin 45 ~ pin 48.

(3) DC ALARM PORT

When Power Unit (4AP) detects low DC voltage, it drives the CN 305 - 5 pin to low, then informs the CPU Card of the DC power condition. The input signal from CN305 - pin 5 is taken as DCALMN from the IC301- *pin 40. This signal normally is "High".*

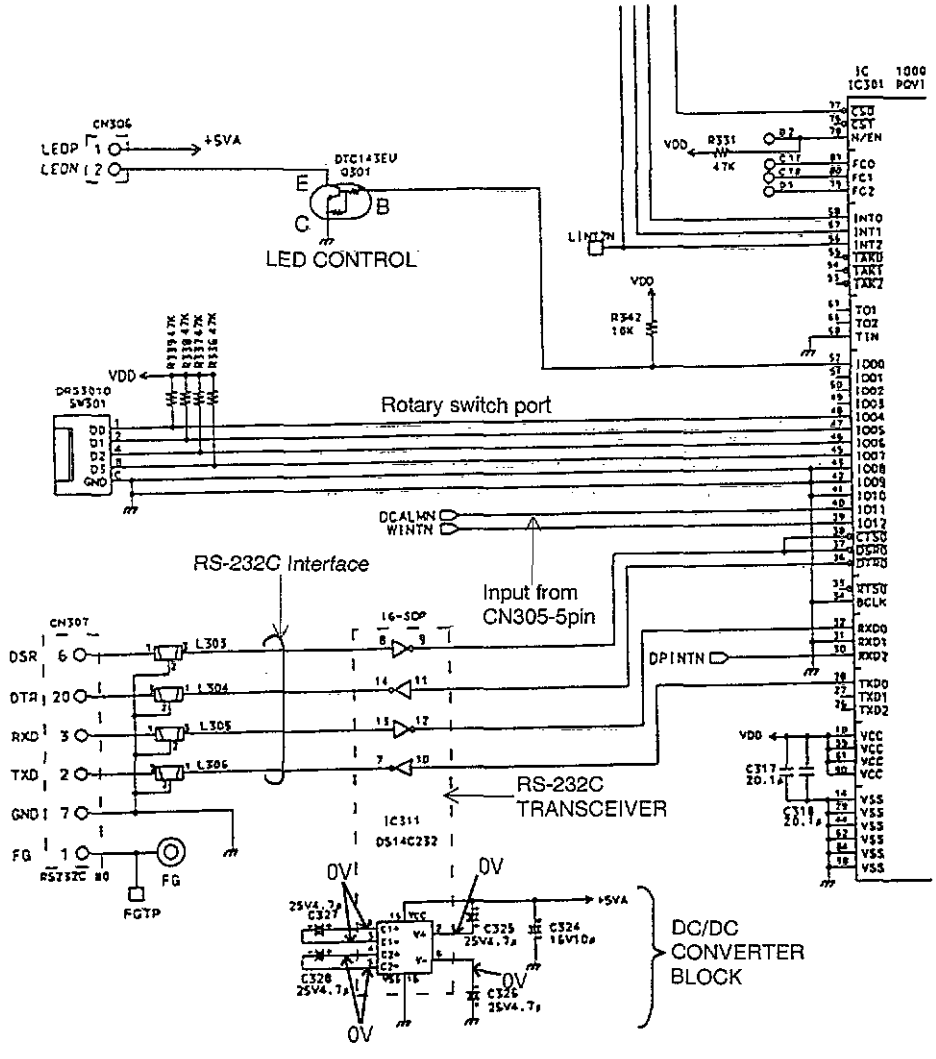


Fig. 4-6. System Port and RS-232C Interface

1-6. *RS-232C interface*

The RS-232C interface is provided by SIO (Serial Input Output Controller) built-in the IC301.

(1) Data Format

When a data character to be transmitted is placed in the SIO, the serial interface automatically adds one start bit before the data bits (lower order bits are output first) and the specified number of stop bits after the data bits. When parity (even, odd) is specified in the mode register, a parity bit is inserted before the stop bit.

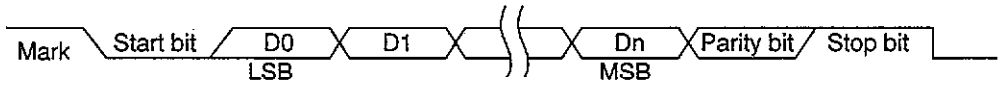
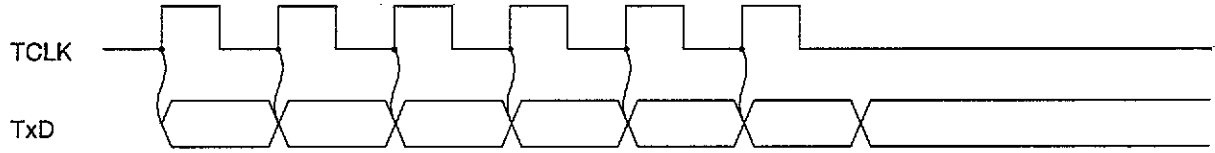


Fig. 4-7. Data Frame

(2) Data Transmission

The Microprocessor checks the DSR (IC301 - 37): Data Set Ready is low, i.e. terminal side's preparation for receiving data finishes, then starts transmission. After transmitting the start bit, the transmit controller automatically appends a parity bit and stop bit to the data character of the specified length and shifts these out to the TxD line. When the next data character has been written to the transmit data buffer, transmission continues with the start bit of the next data character following the stop bit of the current data.

Switchover timing for transmit data bits



TCLK: internal Clock = Baud rate clock.

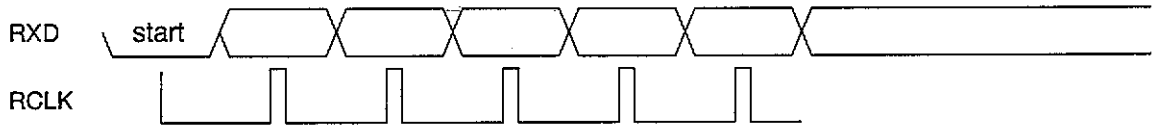
Fig. 4-8. Switchover Timing for Transmit Data Bits

(3) Data Reception

The RxD line is high when no data is in it (mark status). The beginning of a start bit is detected when the input goes low.

For receiving, the first low sampled RXD is detected and, if the sampled data are low for four internal CLKs, this low level is considered to be a valid start bit. The center point of the following data bits is then determined and each data bit is sampled on the TCLK falling edge.

Sampling timing for receive data bits



RCLK: internal Clock = data sampling clock.

Fig. 4-9. Switchover Timing for Receive Data Bits

(4) RS-232C Tranceiver (IC311)

The IC311 is a transceiver IC only for RS-232C. IC311 possesses a built-in DC/DC Converter and generates ±10 V needed for the RS-232C interface. Each terminal voltage of the DC/DC converter block is in Figure 4-6.

1-7. Real Time Clock

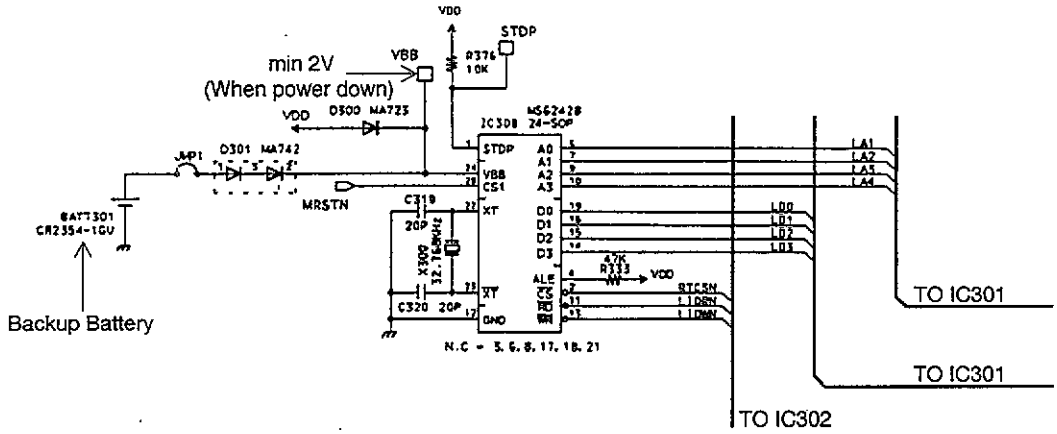
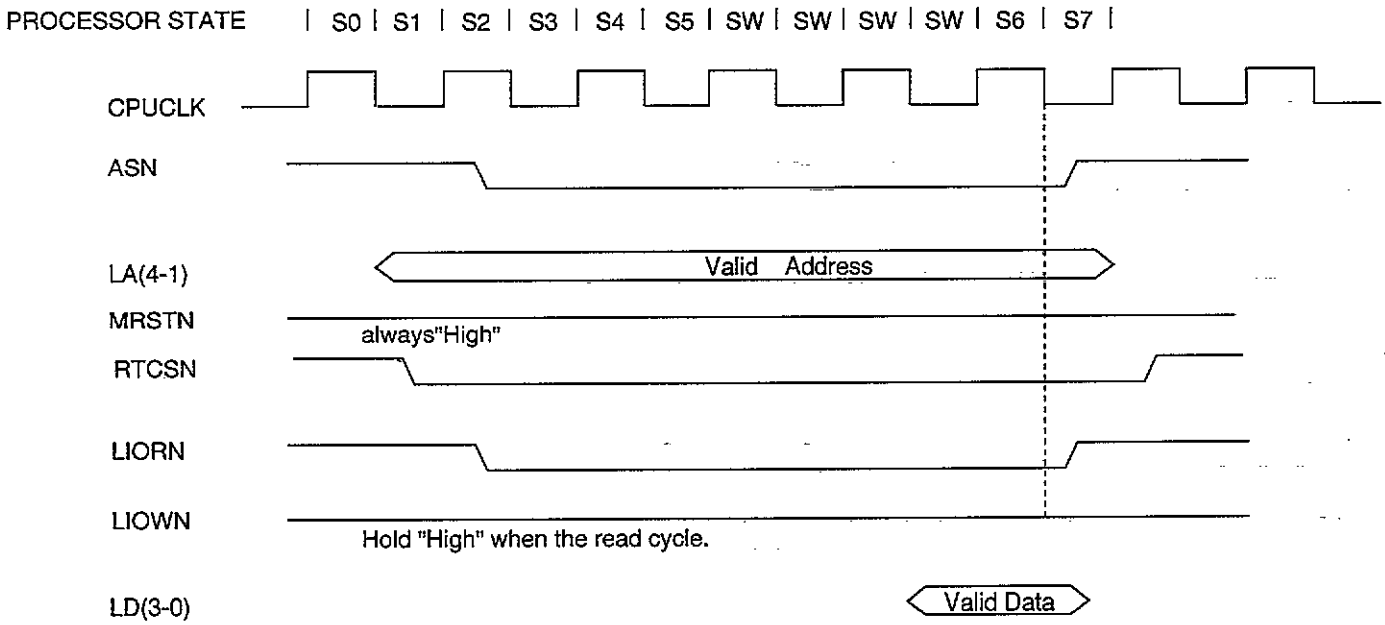


Fig. 4-10. Real Time Clock

The Real Time Clock is provided by IC308. IC308 is a Real Time Clock IC with a fail-safe calender to be able to read and write from seconds. To interface with the Microprocessor four data buses=(LD<3-0>), four address buses=(LA<4-1>), two control buses (LIORN, LIOWN) and two chip select (RTCSN, MRSTN) are needed for set the time/modification/read out.

(1) Microprocessor Read Cycle

Read timing of time data from IC308 by Microprocessor is shown in timing 4-12.

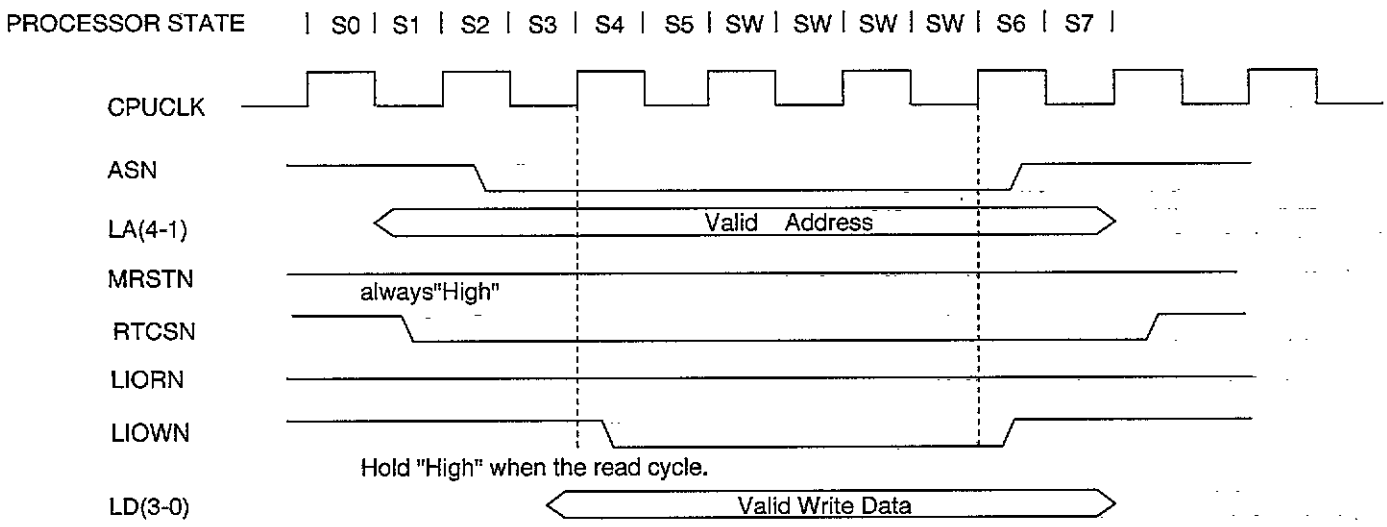


Timing 4-12. Real Time Clock Read by Microprocessor

The Microprocessor (IC301) outputs valid Address to LA(4-1) in S1 state. System Controller (IC302) asserts RTCSN in low. System Controller asserts LIORN to low in S2 state. To Respond to low assertion of LIORN, the IC308 outputs the internal register corresponding with LA(4 - 1). At that time to LD(3 - 0) the Microprocessor takes in effective data on LD(3 - 0) in the falling edge of S6 state.

(2) Microprocessor Write Cycle

Time data's wire timing to IC308 by Microprocessor is shown in Timing 4 - 13.



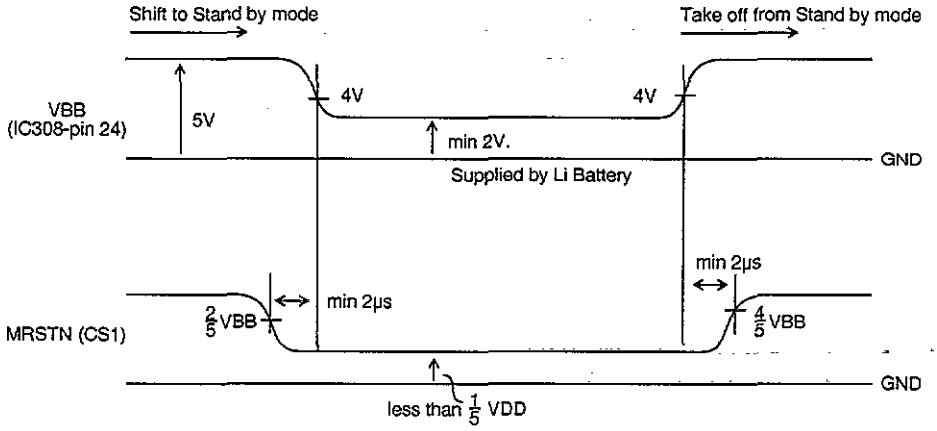
Timing 4-13. Real Time Clock Write Cycle by Microprocessor

The Microprocessor (IC301) outputs Valid Address to LA (4 - 1) in S1 State. System Controller (IC302) asserts RTCSN in low. The Microprocessor outputs Valid Write Data to LD (3 - 0) in S3 state. System Controller asserts in low in time from the rising edge of S4 state to the rising edge of S6 state. IC 308 takes the effective data on LD (3 - 0) in the rising edge of LIOWN.

(3) Battery Back Up Interface

IC308 has two modes: operation mode and standby mode. Operation mode is guaranteed the interface with Microprocessor and is the condition to be able to setting time/modification/read and write.

If provided more than 4/5 of VDD voltage is relayed to the CS1 terminal (pin 20), it becomes the operation mode. If less than 1/5 of VDD voltage is relayed to the CS1 terminal (pin 20), it becomes the stand-by mode. By IC308 checking time function inside IC works but the interface with Microprocessor is not guaranteed. In this mode the consumption of the current decreases. In order to switch over these two modes (operation mode and stand-by mode), The MRSTN signal is connected to the IC308 CS1 terminal.



Timing 4-14. Battery Backup

When Power goes down, MRSTN signal changes the level lower than 2/5 V_{BB} before V_{BB} reaches at 4V. When Power goes up, MRSTN signal changes the level higher than 4/5 VBB after V_{BB} reaches at 4V. With this MRSTN signal, a certain switch over (operation mode and stand-by mode) is guaranteed. In order to guarantee the checking time function of IC308 in stand-by mode, more than 2V voltage should be added to V_{BB}.

This guaranteed voltage is supplied by the lithium battery.

1-8. D-PITS Protocol Controller

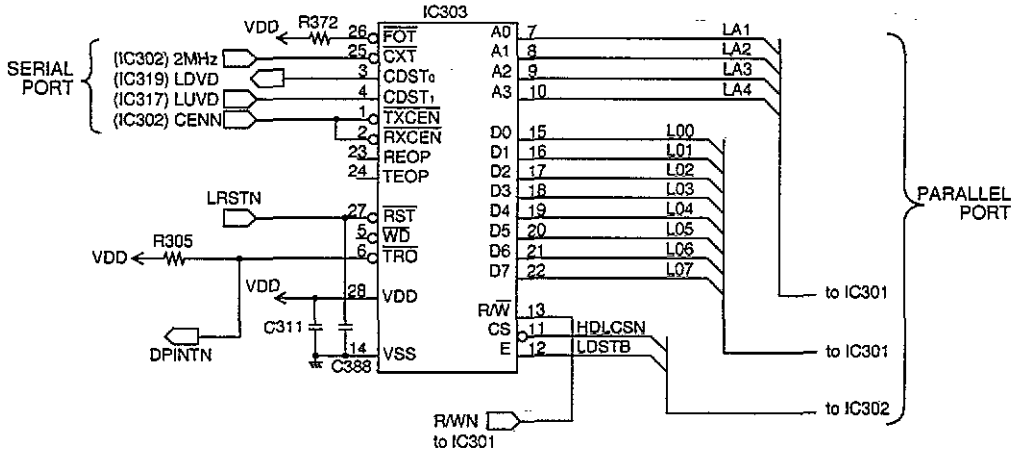


Fig. 4-11. D-PITS Protocol Controller Interface

When Panasonic KX-TD series PBX and VPS are connected, VPS adopts a Data Format and communication protocol based on X.25 (CCITT) level 2 in order to exchange its own status and command parties between the VPS and PBX mutually. This data communication is provided by IC303.

The DPITS Protocol Controller has two ports. The serial port transmits and receives formatted data packets and the parallel port provides a Microprocessor interface for access to various registers in the Protocol Controller.

The Microprocessor Port allows parallel data transfers betwen the Protocol Controller and a Microprocessor bus. This interface consists of Data Bus (LD7 - LD0), Address Bus (LA4 - LA1), Data Strobe (LDSTB), Chip Select (HDLCSN) and Read/Write Control (R/WN). The Microprocessor can read and write to various registers in the Protocol Controller. The DPINTN, active Low output indicates and interrupt requests to Micrprocessor. The interrupt request will be asserted when the packet data transmission is complete or four more packet data receptions are confirmed.

The serial port handles bit oriented protocol structure and formats the data as per the packet switching protocol defined in the X.25 (level 2) recommendations of the CCITT. It transmits and receives the packeted data (information or control) serially as shown in Figure 4-12.

FLAG	DATA FIELD	FCS	FLAG
1BYTE	N Byte (n ≦ 2)	2 Bytes	1 Byte

Fig. 4-12 D-PITS Data Packet Format

Flag:

The flag is a unique pattern of 8 bits (01111110) which defines the frame boundary. The transmit section generates the flags and automatically appends them to the frame to be transmitted. The receive section searches the incoming packets for flags on a bit-by-bit basis and establishes frame synchronization. The flags are used only to identify and synchronize the received frame.

Data:

The data field refers to the Address, Control and Information fields defined in the CCITT recommendations. A valid frame should have a data field of at least 16 bits.

Frame Check Sequence (FCS):

The 16 bits following the data field are the frame check sequence bits. The generator polynomial is:

$$G(x) = x16 + x12 + x5 + 1$$

The transmitter calculates the FCS on all bits of the data field and transmits after the data field and before the end flag. The receiver performs a similar computation on all bits of the received data and FCS fields. The result is compared with $FOB8_{Hex.}$ If it matches, the received data is assumed to be error free.

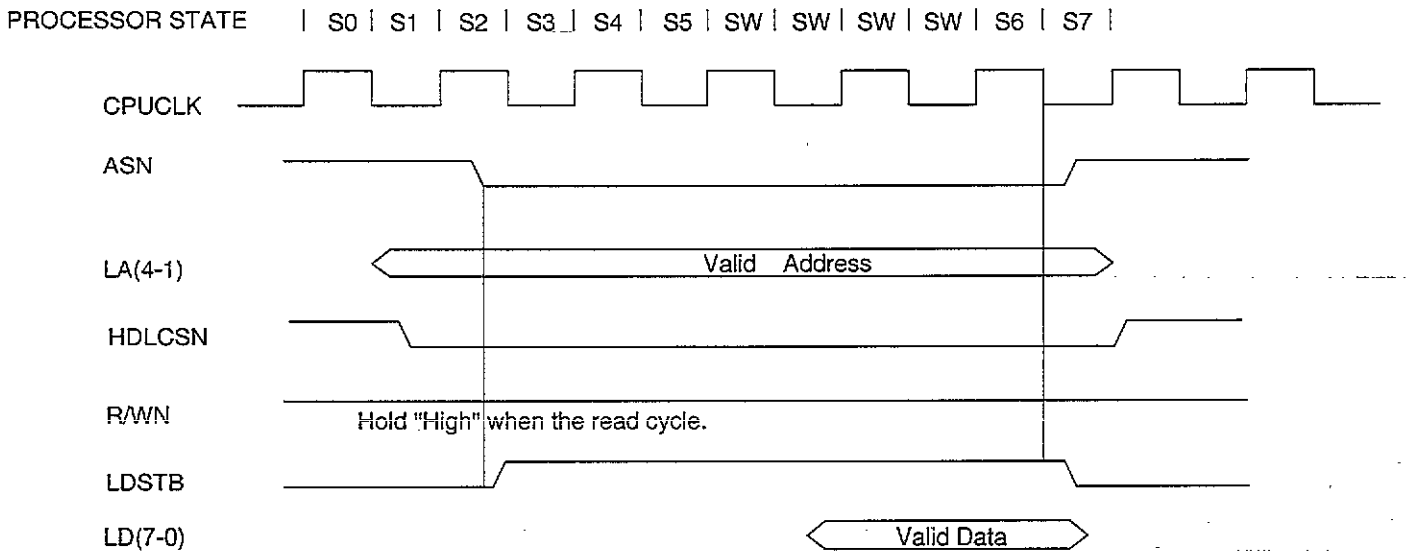
Zero Insertion and Deletion:

The Protocol Controller, while sending either data or the 16 bits FCS, checks the transmission on a bit-by-bit basis and inserts a ZERO after every sequence of five contiguous ONEs (including the last five bits of FCS). This ensures that the flag sequence is not simulated. Similarly, the receiver examines the incoming frame content and discards any ZERO directly following the five continuous ONEs.

In the serial port, the formatted data packets are shifted in/out serially at a rate equal to the clock frequency of 2MHz. The LDVD output is transmitted on the rising edge and the receiver samples the LUVD input on the falling edge of the clock. The CENN controls have effect only after the current bit in the packet is transmitted/received.

(1) Microprocessor Read Cycle

Read Timing internal register of IC303 by Microprocessor is shown in Timing 4 - 15.

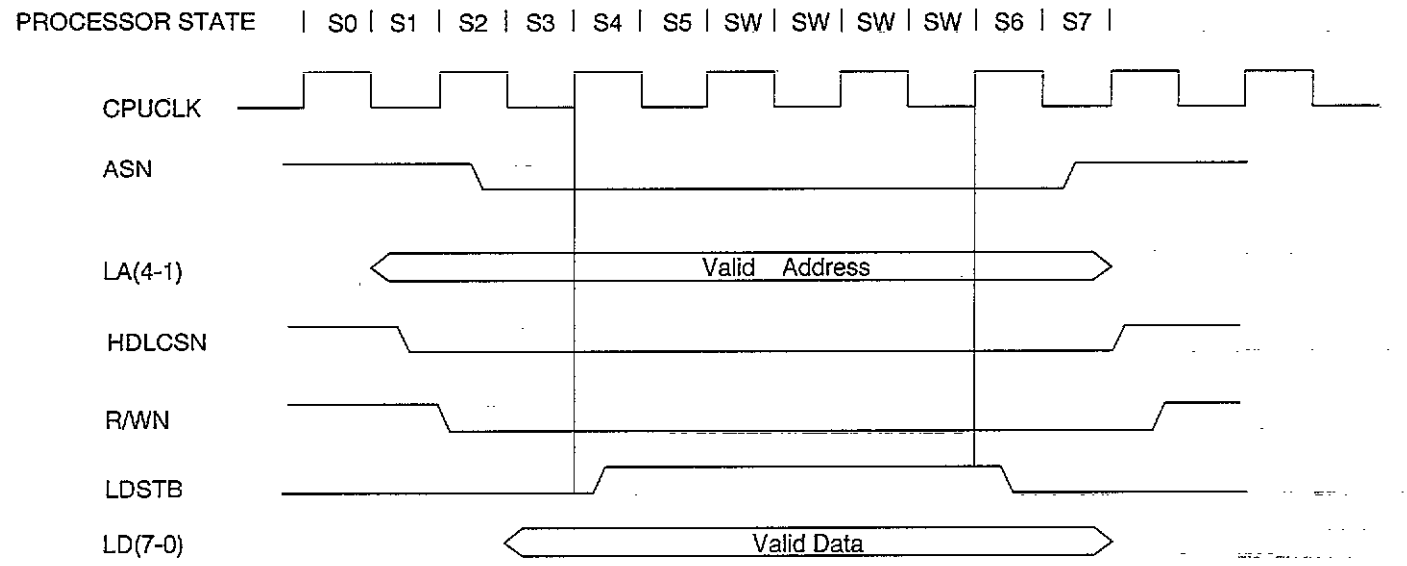


Timing 4-15. D-PITS Protocol Controller Read Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to LA(4 - 1) in S1 state while holding R/WN High. System Controller (IC302) asserts HDLCSN in Low. System Controller asserts LDSTB High in S2 state. LDSTB is asserted in High, R/WN is in High = read condition, IC303 outputs the condition of internal register corresponds with LA (4 - 1) at that time to LD (7 - 0). Microprocessor takes in effective data on LD(7 - 0) in the falling edge of S6 state.

(2) Microprocessor Write Cycle

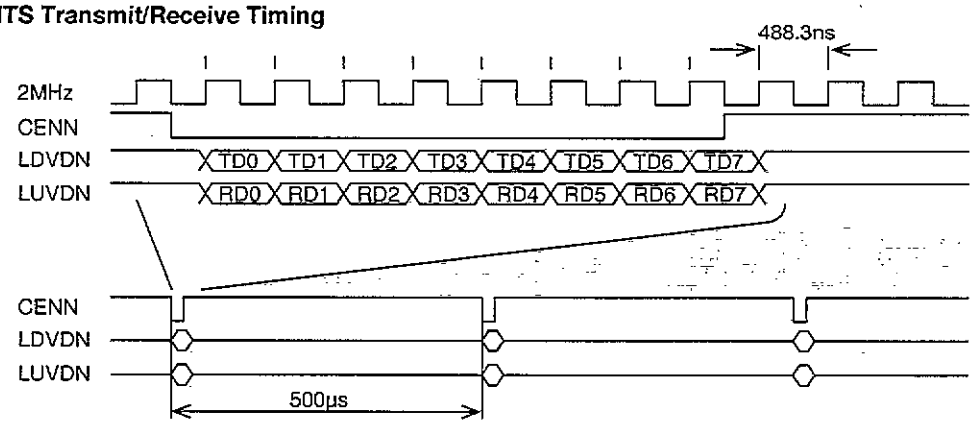
Write Timing internal register of IC303 by Microprocessor is shown in Timing 4 - 16.



Timing 4-16. D-PITS Protocol Controller Write Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to LA(4 - 1) in S1 state. System Controller (IC302) asserts HDLCSN in Low. Microprocessor asserts R/WN in Low = Write in S2 state, then from S3 state it outputs an effective data to LD (7 - 0). System Controller asserts from the period of the rising edge in S4 state to the rising edge of S6 state LDSTB High. IC303 takes in the condition of LA (4 - 1) in the rising edge of LDSTB and writes on the internal register effective data corresponds with LA (4 - 1) internal register in the falling edge of LDSTB .

(3) D-PITS Transmit/Receive Timing



Timing 4-17. D-PITS Transmit/Receive

D-PITS Transmit/Receive Timing is shown in Timing 4 - 17.

D-PITS transmit data (LDVDN) shifted out from IC303 in the rising edge of 2MHz is sent out though IC319 to the DSP card. D-PITS reception data (LUVDN) input from the DSP card is input though IC319 to IC303, then sampled in the falling edge of 2MHz. While an effective D-PITS data exists on the signal line of LDVDN and LUVDN, CENN is asserted in low by the System Controller (IC302).

CENN is asserted by system Controller in the falling edge of 2MHz, and negated in the falling edge after 8 clock cycles. IC303 shifts out effective transmit data to LDVDN in the rising edge of 2MHz. Effective transmit data is from the rising edge of 2MHz right after CENN is asserted to the rising edge right after CENN is negated. Moreover, IC303 samples an effective reception data from the falling edge of 2MHz right after CENN is asserted to the falling edge right after CENN is negated on LUVDN in the falling edge of 2MHz. Data Packet is input and output every 8 bits to the Protocol Controller. The cycle is 500µs.

1-9. Hard Disk Interface

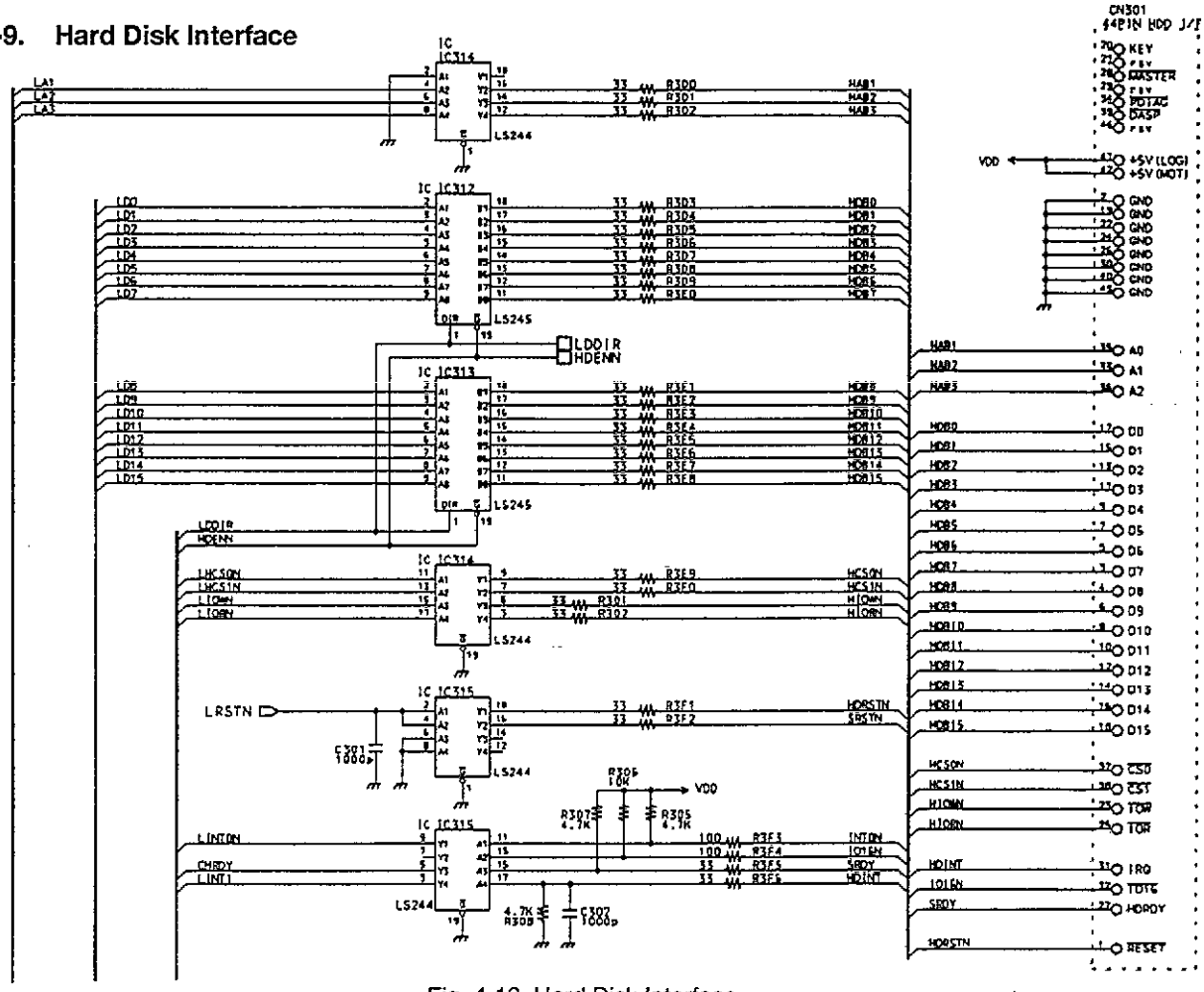


Fig. 4-13. Hard Disk Interface

The Hard Disk Drive used in the VPS installs an intelligent interface built-in disk controller. CPU Card's Interface circuit is shown in Figure 4 - 13. The Hard Disk interface allows parallel data to transfer between the Hard Disk Drive and a Microprocessor bus. This interface consists of a Data Bus (D15 - D0), Address Bus (A2 - A0), Chip Select (CS0, CS1) and 6 control signals (IOR, IOW, IRQ, IO16, HDRDY, RESET). The VPS does not use HDRDY and IO16 signals. The Hard Disk Interface Connector's pin Assignment is shown in Table 4 - 1.

Table 4-1. Hard Disk interface Pin Assignment

Pin No.	Signal Name	Pin No.	Signal Name
1	RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	KEY
21	RESERVE	22	GND
23	IOW	24	GND
25	IOR	26	GND
27	RESERVED	28	RESERVED
29	RESERVED	30	GND
31	IRQ	32	IO16
33	A1	34	PDIAG
35	A0	36	A2
37	CS0	38	CS1
39	DASP	40	GND
41	+5V (LOGIC)	42	+5V (MOTOR)
43	GND	44	RESERVED

(1) Hard Disk Interface Signals Descriptions

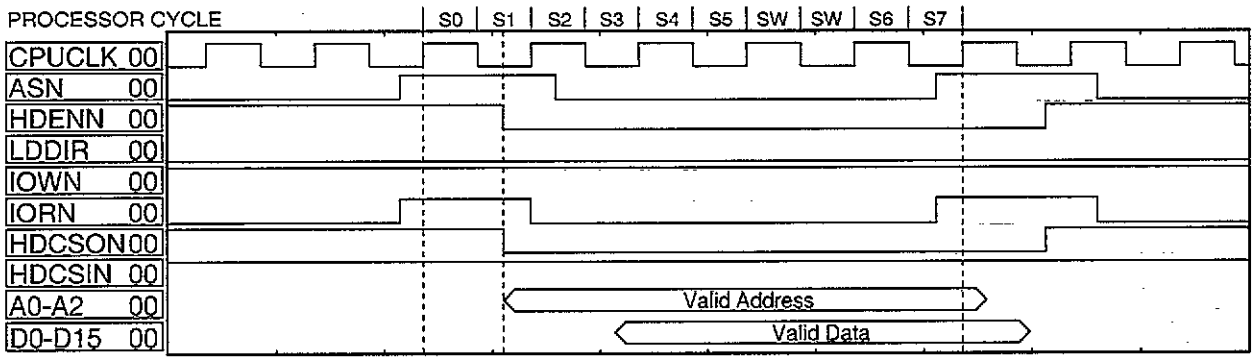
Signal Name	Pin No.	Input/Output	Explanation
-RESET	1	O	Reset signal from host system. Power source of host system turns on, becomes active.
GND	2, 19 22, 24 26, 30 40, 43	O	Ground
DATA 0 - 15	3 - 18	I/O	16 bit mutual direction data bus. Low-ranking 8 bit (DATA 0 - 7) is transferred when it gains access to registers except for the data register and ECC data inside the data register.
KEY Pin	20		Key pin to prevent cable connector from incorrect insertion. on drive side is broken off and removed, then inserted in the pin on the cable side.

Signal Name	Pin No.	Input/Output	Explanation
-IOW	23	O	Write strobe signal. When drive select signal (-CS0.1) is active, data on data bus is written in the register inside drive by the Trailing Edge.
-IOR	25	O	Read strobe signal. When drive select signal (-CS0.1) is active, data inside the register is output onto the data bus with low active, then it is read into the host system with Trailing Edge.
IRQ	31	I	Interrupt signal to host system. It is active when drive is selected, and -IEN (Interrupt Enable) inside flexed disk register is active. Generated interrupt phenomenon or not it becomes high- impedance status except when the above condition occurs. IRQ signal is reset when host system reads status register or command is written in the command register.
RESERVED	21, 27 28, 29 44		Reserve Signal. Non-connecting condition.
-IO16	32	I	The signal (Open drain) informs the 16 bit data transferred mode (16 bit data register is gained access). (Not used)
-PDIAG	34	I/O	Used to inform master drive of the existence of slave drive and to receive and send the result of the diagnostic com mand between the master and slave drive. (Not used)
A0, A1, A2	35, 33, 36	O	Address decode signal of internal register.
-CS0	37	O	Chip select signal. To select one group within two internal register groups.
-CS1	38	O	Chip select signal. To select one group within two internal register groups.
-DASP	39	I	During drive access (from receiving command to command end), it becomes active. Used to drive external LED. Composing Master/slave, it is used to inform master drive of the existence of the slave drive. (Not used)
+5V (LOGIC)	41	O	Power source of logic group • analog group
+5V (MOTOR)	42	O	Power source of motor driving.

* The signal from drive to host system is I (Input), from host system to drive is O (output).

(2) Microprocessor Read Cycle

Read Timing from the internal register of the Hard Disk by Microprocessor is shown in Timing 4 - 18.

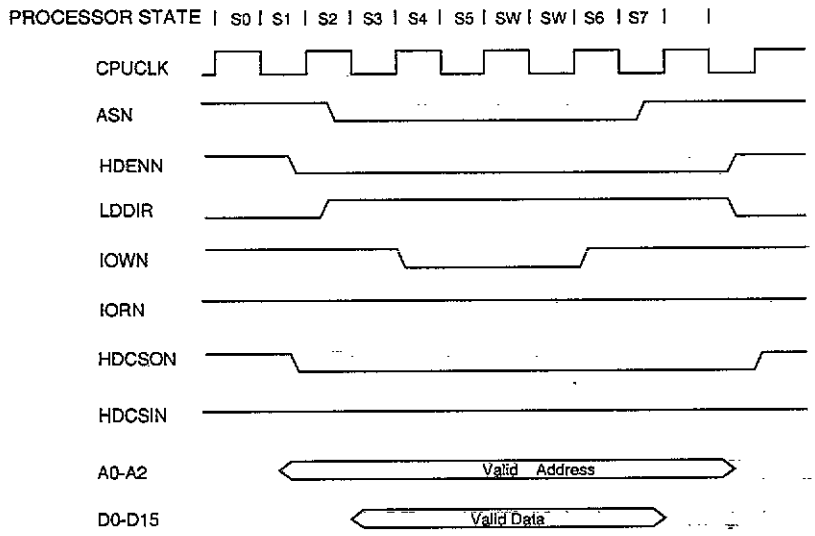


Timing 4-18. Hard Disk Read Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to A(2 - 0) in S1 State. System Controller (IC302) asserts either HDCSON or HDCSIN. System Controller asserts IORN low in S2 state. Hard Disk outputs the condition of internal register correspondence with A(2 - 0) IORN in time IORN is asserted to D(0 - 15). The Microprocessor takes effective data on D(15 - 0) in the falling edge of S6 State. In Read Cycle, IC312/IC313 (L5245 Bus Tranceive) is the Control Signal. HDENN (IC312/IC313, pin 19) is asserted in low in the period from S1 state to S7 state. LDDIR (IC312/IC313, pin 1) is asserted in low.

(3) Microprocessor Write Cycle

Write Timing to the internal register of the Hard Disk by Microprocessor is shown in Timing 4 - 19.



Timing 4-19. Hard Disk Write Cycle by Microprocessor

Microprocessor (IC301) outputs Valid Address to A(2 - 0) in S1 State. System Controller (IC302) asserts either HDCSON or HDCSIN. Microprocessor outputs effective written data onto D(15 - 0) in the period from S3 state to S7 state. System Controller is asserted in low in the period from the rising edge of S4 state to rising edge of S6 state. Hard Disk takes effective data on D(15 - 0) inside by the rising edge of IOWN. In Write Cycle HDENN(IC312/IC313 - pin 19) , Control Signal of IC312/IC313 (LS245 Bus Transceiver), is asserted in low in the period from S1 state to S7 state. LDDIR (IC312/IC313 - pin 1) is asserted in low in the period from S2 state to S7 state.

1-10. Extension Bus (DSP Card Interface)

The Expansion Bus has two ports. The serial port transmits and receives the voice data and the parallel port provides a Microprocessor interface for access to various registers in the add-in card. The CPU Card distributes the Bus signals to 3 expansion connectors (CN302, CN303, CN304).

(1) Add in Card Selection Signals

The CPU Card provides these connectors Slot ID Signal composed by S(2 - 0). SL(2-0) is used in case of gaining access to add-in Card mounted by Expansion Connector, to select a card from others. The Add-in Card mounted to Expansion Connector compares the value of SL(2 - 0) provided from the connector with a part of destination address = ESA(2 - 0) provided by Microprocessor. The result of the comparison is considered by the add-in card condition of card selected. In this VPS, "000" for CN304 = slot 1, "001" for CN303 = slot 2 and "010" of slot IC = SL(2 - 0) for CN302 = slot 3 are provided.

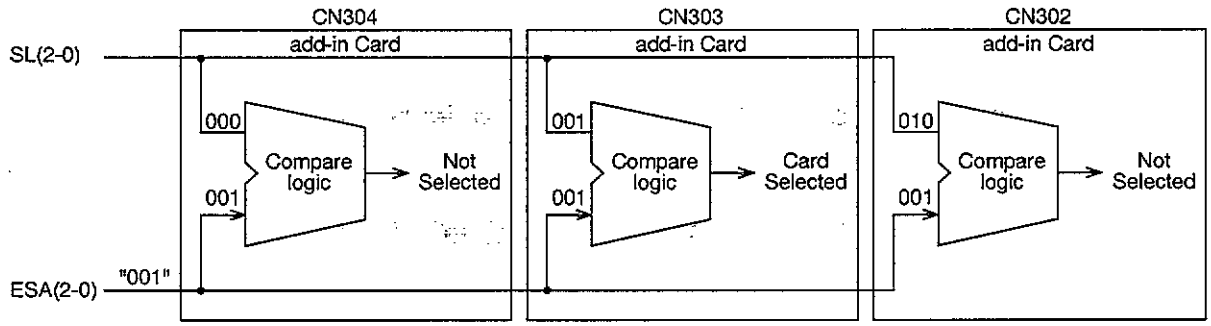


Fig. 4-14. Card Selection Logic for the Expansion Bus

(2) Microprocessor Port

The Microprocessor Port allows 8 bit parallel data transfers between the various registers on the add-in card and a Microprocessor on the CPU Card. This interface consists of a Data Bus(DB7 - DB0), Address Bus (AB6~AB1) Card Select (SL(2 - 0), ESA (2 - 0), IOSN), 2 Control Signals (LDSN, RWN) and 3 miscellaneous signals (SRSTN, IORDY, INTON, SCLK). Table 4 - 2 describes the Microprocessor Port.

Table 4 - 2. Microprocessor Port of the Expansion Bus

Signal Name	Pin No.	Input/Output	Explanation
DB (7 - 0)	10 ~ 3	I/O	8 bit bidirectional Data Bus. This data bus allows data transfer between I/O port in the add-in Card and a Microprocessor.
AB (06 - 01)	18 ~ 13	O	6 bit output Address Bus. These bits address the various registers in the add-in card. They select the internal registers in conjunction with card select and control signals.
ESA (2 - 0)	23 ~ 21	O	3 bit expansion Slot Address Bus. These bits address one expansion Slot within other expansion slots.
SL (2 - 0)	36 ~ 34	O	3 bit expansion slot identity output. These bits are given to each expansion slot. It shows a unique slot number.
IOSN	24	O	Card Select output. This is an active low output, enabling the read or write operation to various registers in the add-in card.
LDSN	27	O	Lower byte Strobe output. This output activates the Address Bus and RWN output and enables data transfers on the Data Bus.
RWN	28	O	Read Write Control output. This output controls the direction of data flow on the data bus. When High, the I/O buffer acts as an output drive and as an input buffer when low.
SRSTN	33	O	System Reset Output. This is an active low output, resetting all the registers in the add-in card.
INTON	30	I	Interrupt Request input.(Open Collector) This active low input notifies the controlling Microprocessor of an interrupt request.
IORDY	29	I	IO Data Ready input (3 state) This active High input indicates the current bus cycle is complete. If the add-in card negates this signal at the current bus cycle, when the Microprocessor addresses the slower device on the add-in card, the current bus cycle waits until IORDY asserts to High.
SCLK	37	O	System Clock output. This clock output is the same as SPUCLK (12.288MHz).

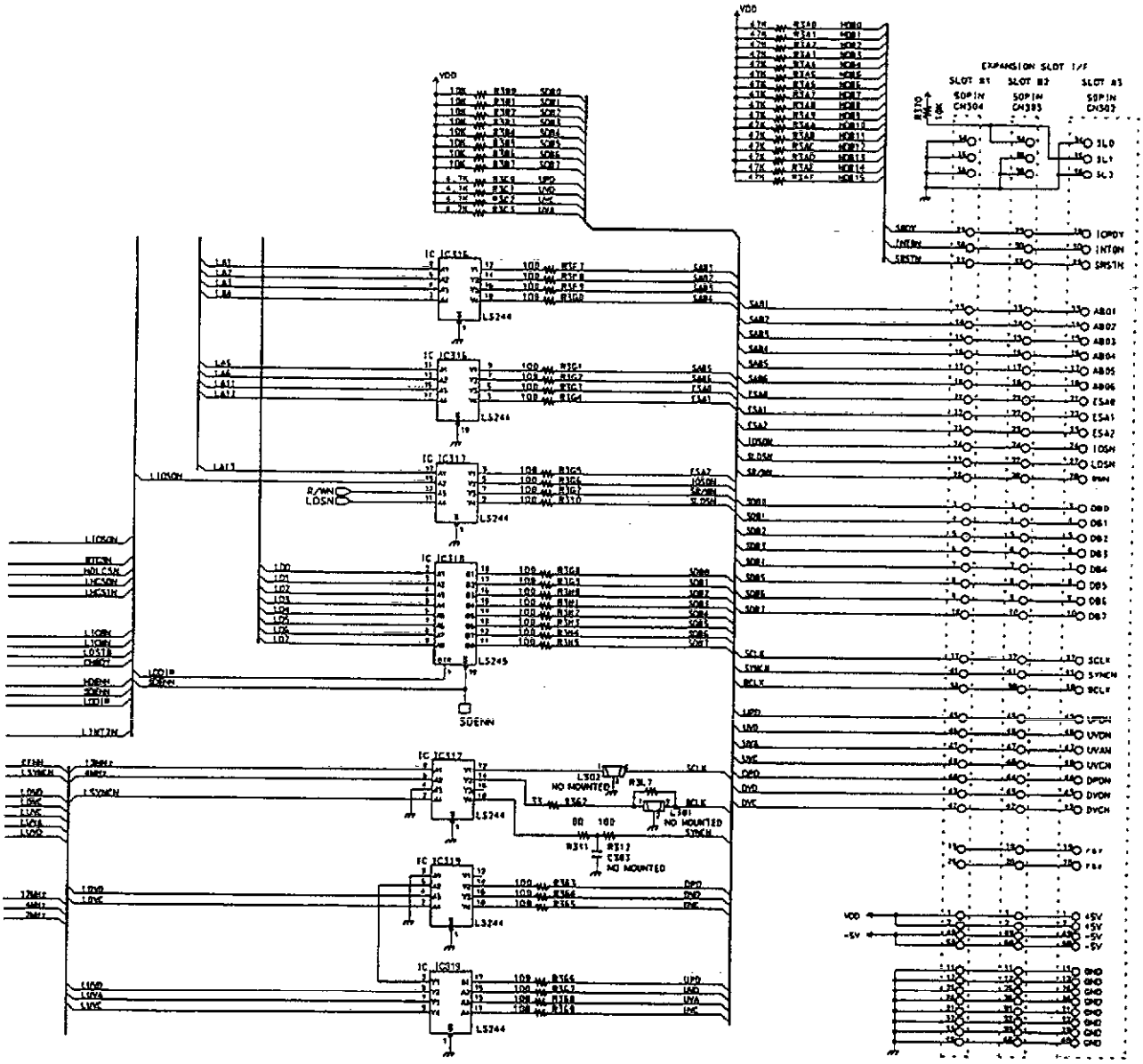
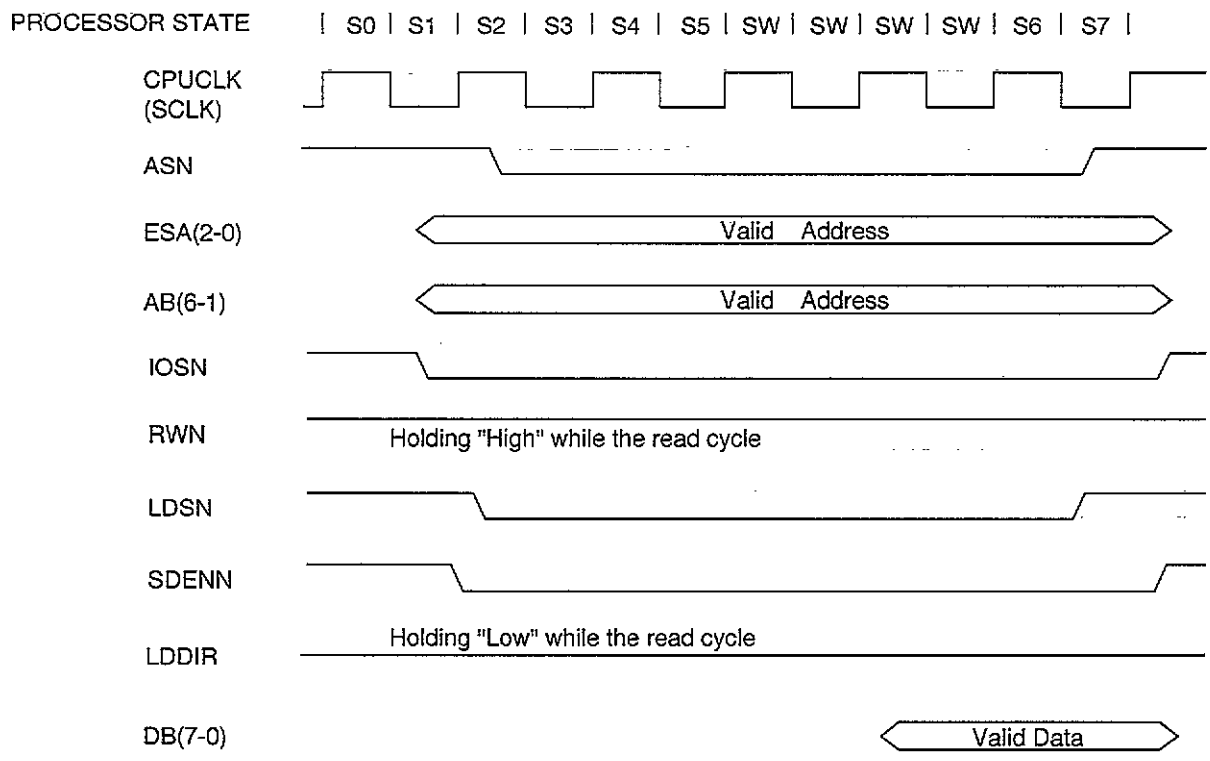


Fig. 4-15. Expansion Bus Interface

(3) DPS Card Read Cycle By Microprocessor

Read Timing of the DSP Card by Microprocessor is shown in Timing 4 - 20.



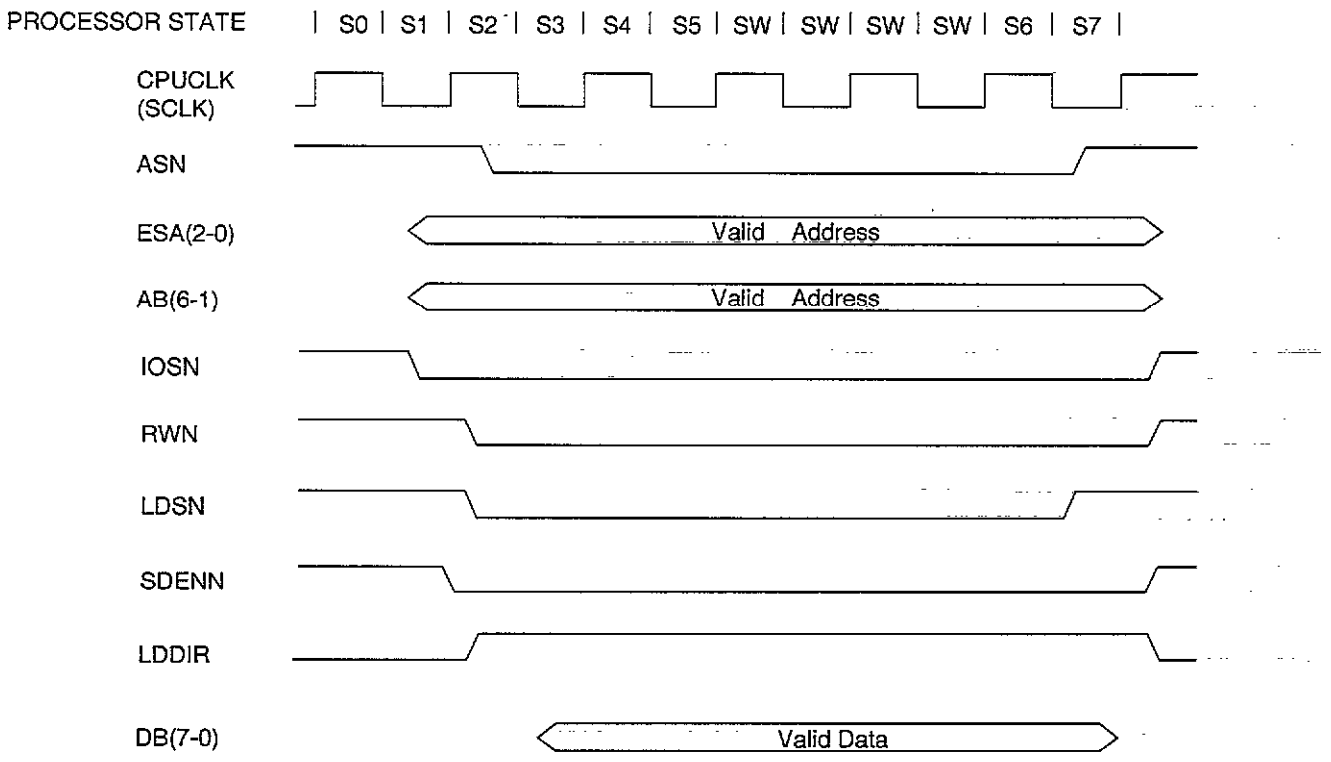
Timing 4-20. DSP Card Read Cycle by Microprocessor

The Microprocessor (IC301) outputs Valid Address to ESA (2 - 0) in S1 State. System Controller (IC302) asserts IOSN in low. Microprocessor holds RWN High, asserts LDSN in low, in the period from the rising edge of S2 state to the falling edge of S6 state. DSP card outputs the register condition corresponding with AB (6 - 1) and ESA (2 - 0) to DB (7 - 0). Microprocessor takes effective data on DB (7 - 0) in the falling edge of S6 state. In Read Cycle SDENN (pin 19), control signal of IC318 (LS245 - Bus Tranceiver) is asserted by system controller in the period from S1 State to S7 State in low. LDDIR (1 pin) is asserted in low.

(4) DPS Card Read Write By Microprocessor

Write Timing of DSP Card by Microprocessor is shown in Timing 4 - 21.

Microprocessor (IC301) outputs Valid Address to AB (6 - 1) and ESA (2 - 0) in S1 State. System Controller (IC302) asserts IOSN in low. Microprocessor asserts RWN in S2 State in low, and outputs write data from S3 state onto DB (7 - 0). Microprocessor asserts LDSN in lo w in the period from the rising edge of S2 state to the falling edge of S6 State. DSP card takes effective data on DB (7 - 0) in the rising edge of LDSN. In Write Cycle SDENN (pin 19), control signal of IC308 (LS245 - Bus Tranceiver) is asserted by the system controller in the period from S1 State to S7 State in low.



Timing 4-21. DSP Card Write Cycle by Microprocessor

(5) Overview of the Serial Voice Port

Voice Port lessens the connecting signal line between the CPU and DSP Card. This time-share serial bus is designed to realize transmitting sufficient data in its performance. The Control section on the host (CPU) side is the master controller and the control section on the DSP card side is the slave controller.

Data for two kind of 32 channels passes through on this bus. Data types are ADPCM VOICE Data (32kBPS/CH) and D-PITS Data (max 32kBPS/CH). The Time slot passes through individual data called VOICE Channel and PITS Channel.

•Voice Channel

Voice Channel is a serial bus with bit rate : 2MHz and practice data transfer ability : 32 kBPS, and each individual channel is in the 32 time- share. Normally ADPCM compressed voice data is passing through.

DMA data transfer method is offered by Voice Channel. The cooperation DMA channel inside the slave controller and bus masterlogic inside the master controller makes it possible for DMA data between the voice buffer inside the controller and host memory to transfer.

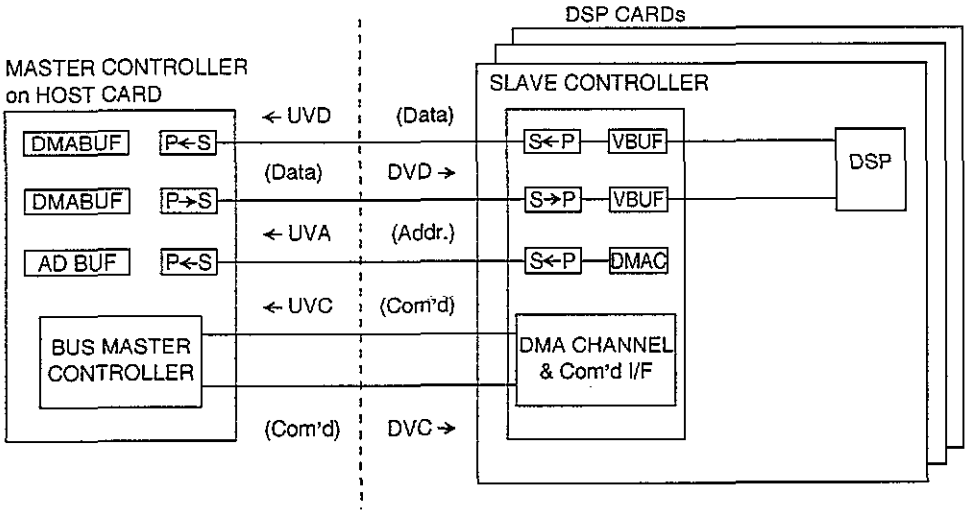


Fig. 4-16. Voice Channel on the Voice Port

In DSP/COL Card Module, voice Band digital data is received from the circuit : T-R line is input by DSP, and DSP executes voice data's ADPCM compressing disposition. Compressed ADPCM data is stored in the voice buffer inside the slave controller by DSP. Voice Channel transfers DMA to host memory by the speed of 32kBPS/channel.

In time recording disposition (voice compression) ADPCM data stored by DSP in the voice buffer inside the slave controller, data transfer and address information, and DMA channel inside the slave controller, are output to the voice channel. Based on this information, master controller drives inside its bus master logic, holding CPU, then stores ADPCM data input from Voice Channel on host memory.

In play-back disposition, ADPCM data on host memory is stored in the voice buffer inside the slave controller from the voice channel. ADPCM data inside the voice buffer is restored to voice band digital data by DSP, and sent out to the line : T-R line.

In this playback disposition, data transfer information and address information generated by the DMA channel inside the slave controller are output to the voice channel. Based on this information, master controller drives in its bus master logic, holding CPU, then transfers ADPCM Data from host memory to the Voice channel buffer inside master controller. The data stored in the Voice channel buffer is transferred to the VOICE channel buffer inside the master controller through the voice channel. DSP takes over ADPCM from this voice buffer.

•PITS channel

PITS Channel is a time-share bus of 2MBPS and 16 bitx32channels. It realizes transmitting data between D-PITS buffer inside the slave controller and HDLC controller on the CPU card. The data, sent and received in D-PITS buffer inside the slave controller through the PITS channel, is sent and received by the PBX through interface logic.

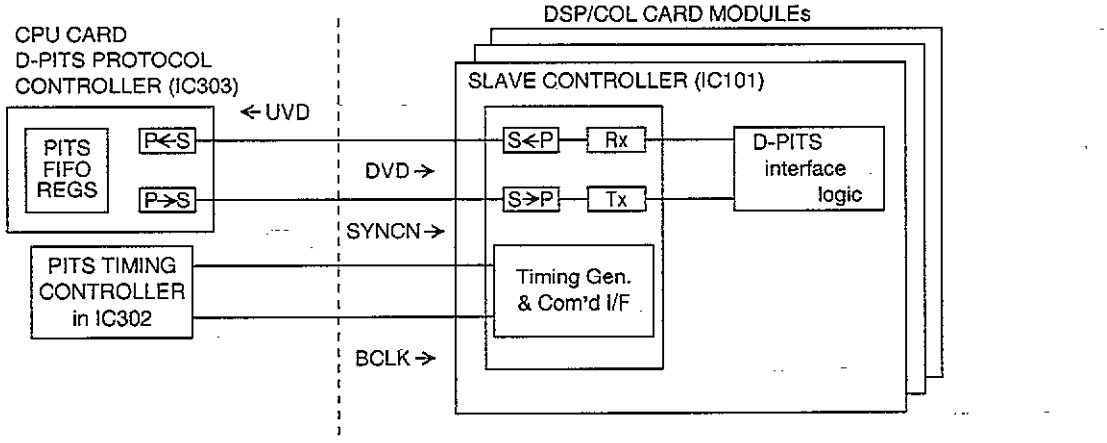


Fig. 4-17. PITS Channel on the Voice Port

When receiving and sending D-PITS data, data transfer between the D-PITS protocol controller (IC303) on the host card and the PITS buffer inside the slave controller (IC101) is realized. PITS control logic inside the master controller (IC302) controls the receiving and transfer timing of the D-PITS protocol controller on the host card. The data channel component is extracted from the D-PITS data received from the circuit line by interface logic, then stored in the PITS-RX buffer inside the slave controller. D-PITS data stored in the PITS-RX buffer inside the slave controller is input in the D-PITS protocol controller on the host card through the PITS channel. The PITS-RX buffer size inside the slave controller is 8 bit.

D-PITS data to be sent out from the circuit line is stored in the PITS-TX buffer inside the slave controller from the D-PITS protocol controller through the PITS channel. D-PITS data stored in the PITS-TX buffer is symbolized by interface logic and output from the circuit line. The PITS-TX buffer size inside the slave controller is 8 bit.

(6) The Frame Format of the Voice Port

Voice Port is composed by five lines, SYNCN (Synchronization pulse) directs master controller → slave controller (down road), BCLK (Bit Clock), DVD (Download-Voice-Data), DVA (Download-Voice Address) and DVC (Down load-Voice command), two signal lines, and UVD(Upload-Voice-Data) directs master controller (up load) and UVC (Upload-Voice-Command).

Master controller outputs frame pulse (SYNCN : 2kHz) and Base Clock (BCLK : 4.096MHz) to the slave controller for synchronization.

Voice Port is 500us/32 channel time share bus, synchronized with SYNCN generated from the Master Controller. One frame of the voice port is 500us and VOICE/PITS DATA of 32 channels pass through time share. VOICE/PITS DATA maximum 1x32 channel/frame can pass through one frame period. Each VOICE Channel/ PITS channel is composed of 488ns/bit (2.048MHz) x 16bit (=7812ns), the arrangement of each channel is from the head VOICE channel:0, PITS channel:0, VOICE channel:1, PITS channel1, ..., VOICE channel:31, PITS channel :32.

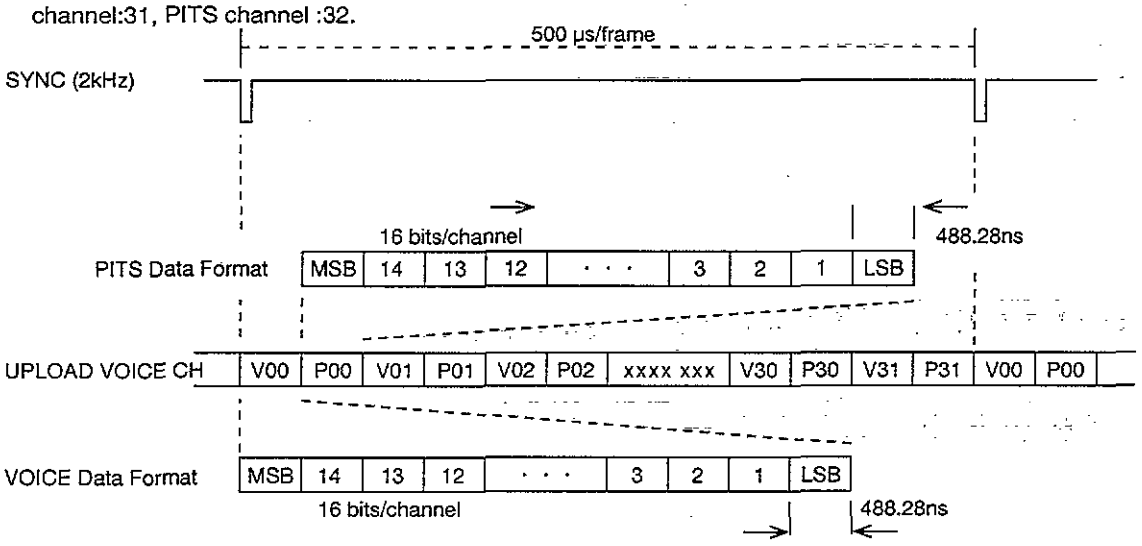


Fig. 4-18. Voice Port Timeslot Assignment

Host CPU programs the slave controller. The slave controller assigns the channel which can be used. Time slot logic inside the slave controller, corresponds with this channel assignment, decides the channel slot available for itself and make required control signals from the frame pulse and 4MHz clock.

In VOICE channel, down load timing is behind the time for 64 bit (31.24usec) in regard to up load timing. Voice channel offers a DMA transmitting method. For this reason, command reception of the master command and latency for direct memory access are added.

In case of down loading play back data from the host memory to the DSP card using DMA data transfer; eg, VOICE data, responded to DMA data transfer command up-loaded in CH0, is down loaded in the timing of CH2. VOICE channel defines each channel, up-loaded at the time SYNC is being asserted, as CH0, thereafter, CH1, CH2,...CH31.

PITS channel has no DMA data transfer function. Referring to external-fixed HDLC controller and interface, up load channel and down load channel are the same timing.

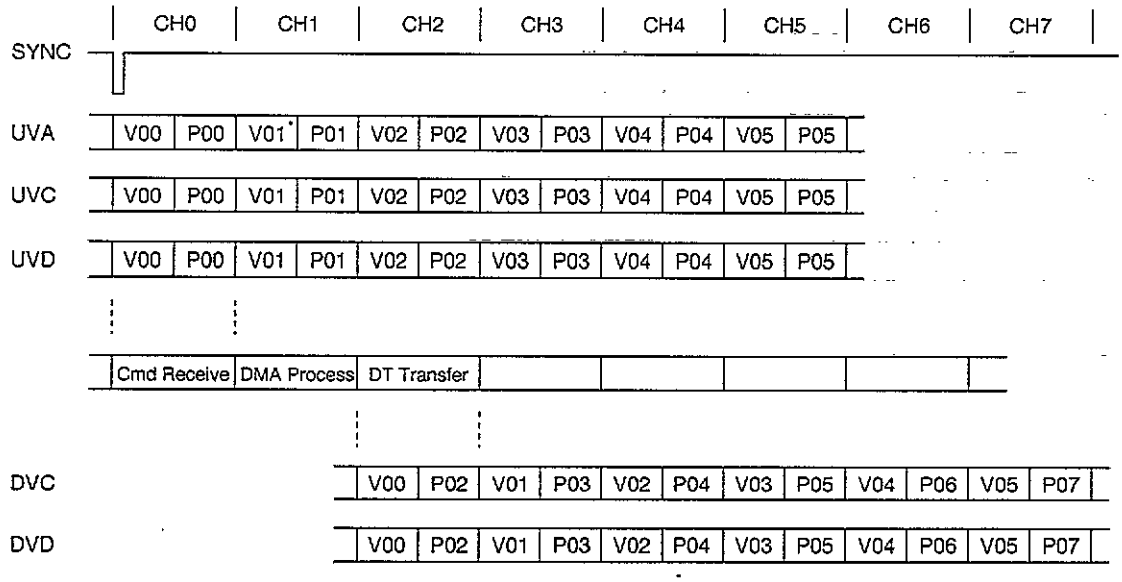


Fig. 4-19. Voice Port Frame Format

(7) The Data Format of the Voice Port

•VOICE CHANNEL Data Format

Format of the VOICE channel in up load channel is defined as follows.

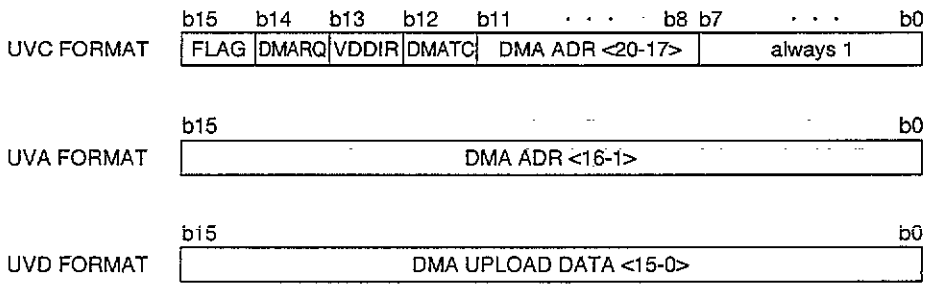


Fig. 4-20. Voice Channel Upload Data Format

FLAG bit of command channel is a signal that indicates the DMA channel inside the slave controller to start transmitting effective data and Low assert.
DMARQ bit is a DMA request signal, against the DMA channel inside the slave controller. It asserts when DSP on the DSP card requests host memory to transfer DMA data and it is in Low assert. The Master controller motivates the DMA data transfer process for the channel and its main bit is asserted.
DMATC bit is a TC (Transfer Complete) signal asserted when the number of times the DMA channel inside the slave controller executed, reaches the regulated number of times and low assert. This bit is asserted only once when it reaches TC, this bit is latched the inside master controller and informed to the host CPU as a DMATC intrusion.
DMA ADR(20 - 1) bit, divided in the command and address channel, is an address on system memory existing as ADPCM data.
DMA DATA (15 - 0) allotted to the data channel is up load data to be a DMA object. This data is ADPCM voice data to be stored in system memory, compressed on the DSP card.

The mode of DMA can be divided into two groups because of the direction of the DMA transfer.

First, in the case of the DSP card → host memory; data is transferred from a 16 bit voice buffer inside the slave controller to a DMA data buffer inside the master controller. The Slave controller is asserted as DMARQ to command channel, DMA address is placed on the address channel, and data is placed on the data channel. Then these are transferred to the master controller. Master controller stores transferred command/ address/data in a DMA buffer temporary, then requires the host CPU to hand over Bus Ownership. When host CPU releases, the bus master controller executes a transfer from DMA buffer to host memory.

Second, in the case of host memory → I/O card, data is transferred from a 16 bit DMA data buffer inside the slave controller to a voice buffer inside the I/O card. Slave controller is asserted as DMARQ to the command channel, DMA address is placed on the address channel, then these are transferred to master controller. Master controller stores transferred command/address/data in a DMA buffer temporarily, then requires the host CPU to hand over Bus Owner ship. When host CPU releases, the bus master controller reads data from the host memory, in the next phase through up load bus transfers data to slave control.

Mode phase of the VOICE channel by up load command is as follows.

TYPE OF UPLOAD COMMAND				
DWAIT	DMARQ	VDDIR	DMATC	FUNCTION
0	0	0	1	HOST → I/O CARD DMA Request
0	0	1	1	I/O CARD → HOST DMA Request
0	0	0	0	HOST → I/O CARD DMA Request with TC flag
0	0	1	0	I/O CARD → HOST DMA Request with TC flag
1	x	x	x	idle State

Format of down load channel is defined as follows.

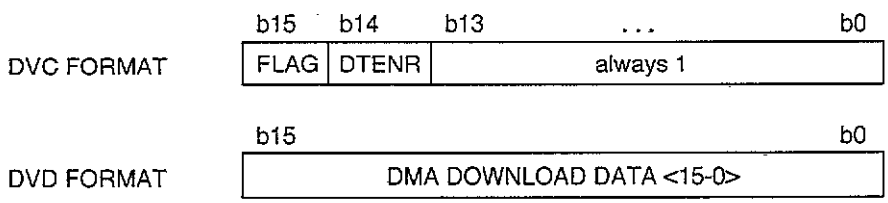


Fig. 4-21. Voice Channel Download Data Format

The Down load channel has only a command channel and data channel.
FLAG bit of the command channel is a signal indicating the master controller to start effective data transfer, and low assert.
The meaning of DTENB bit differs with the direction of data transfer.
In master controller→slave controller direction transfer; it is indicated that data on the data channel sent by the master controller is the same as the data on the host memory requested from the DSP card.
Slave controller→master controller direction controller, it is indicated that effective data sent from the slave controller is stored in system memory. This bit is low assert.

DMA transfer direction is host → DSP card; the effective data should be transferred from a 16 bit DMA data buffer inside the master controller to a voice buffer inside the slave controller. Master controller stores DMA address sent from the DMA channel inside the slave controller together with a DMA request in the DMA buffer temporarily, then requires host CPU to release bus. When host CPU releases, master controller reads data from host memory, then transfers effective data to the slave controller through the down load channel in the following phase.

Motion phase of VOICE channel by down load command is as follows.

TYPE OF DOWNLOAD COMMAND		
START	DMAEN	FUNCTION
0	0	Requested DMA Transfer Succeed
1	x	idle State

•PITS CHANNEL data Format

PITS channel uses only data line and its format is defined as follows.

	b15 b8	b7 b0
DVD FORMAT	D-PITS DOWNLOAD DATA <7-0>	not defined
UVD FORMAT	D-PITS UPLOAD DATA <7-0>	not defined

Fig. 4-22. PITS Channel Data Format

DATA (7 - 0) allotted to the down load channel indicates D-PITS DATA to be sent to the PBX, DATA (7 - 0) allotted to the up load channel indicates D-PITS data received from the PBX.

KX-TVP100E

■ MEMO

2. DSP CARD

2-1. Overview of the DSP CARD

Circuit Diagram of DSP Card is shown in Figure 4-23.

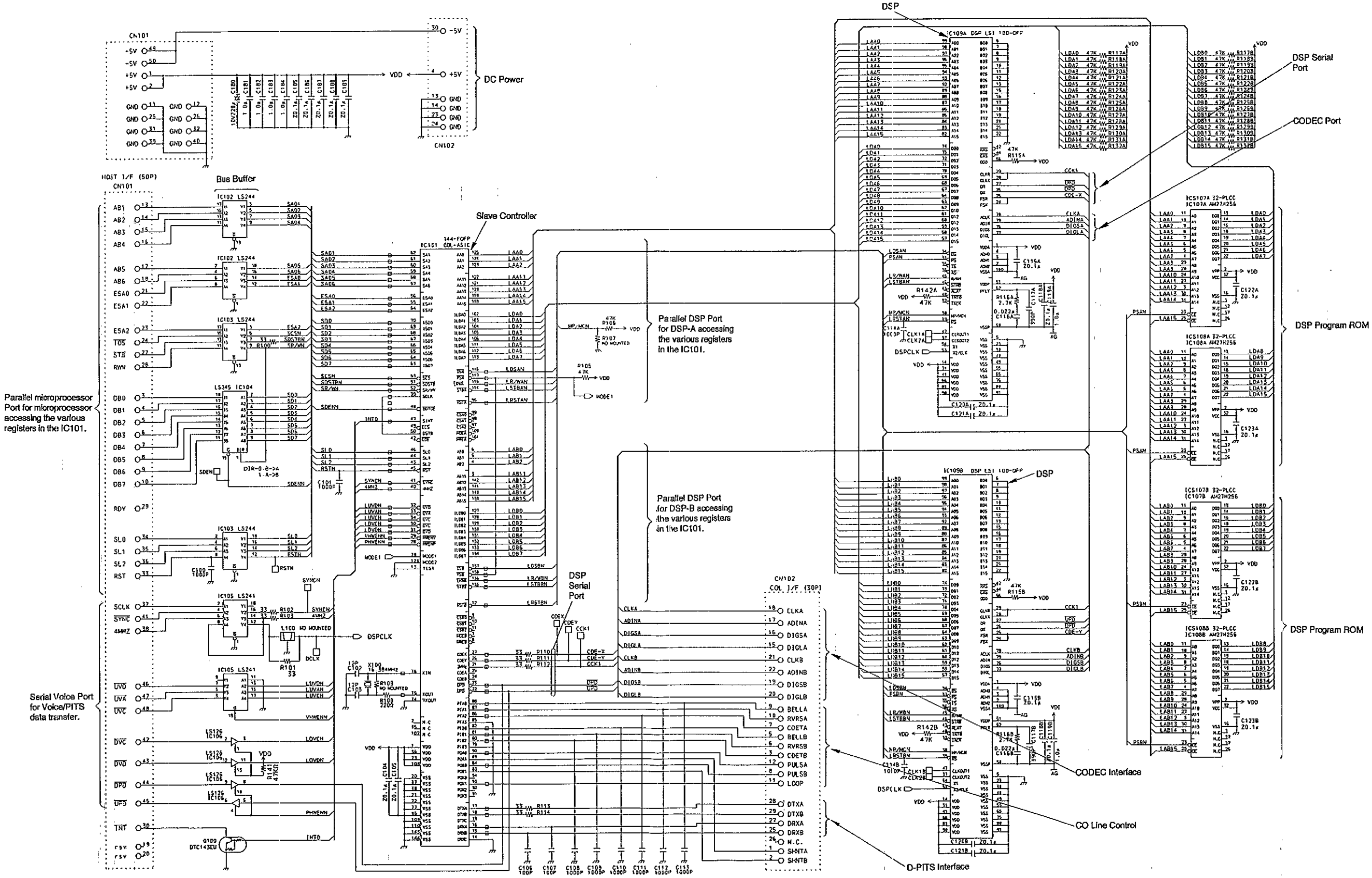


Fig. 4-23. Schematic Diagram of DSP Card

The function of the DSP Card is integrated in the Slave Controller (IC101) and DSP (IC109). These LSI devices include the functions mentioned below.

Slave Controller
- •FIFO to communicate between Microprocessor and DSP.
- •Voice Port Interface to transfer ADPCM data between system memory and DSP.
- •D-PITS interface to receive and send digital data by D-PITS protocol.
- •Line interface control I/O port to detect BELL, off-hook control, etc.

DSP (IC109)
- •Compression/extension of voice data by ADPCM algorithm.
- •To detect and generate DTMF.
- •To detect and generate TONE.
- •Detection of VOX (no-sound) condition. (To detect the condition of completed conversation.)
- •Automatic gain adjustment of recording level.

2-2. CPU Card Interface

Refer to section 1-10. Expansion Bus.

2-3. DSP Clock

4.096MHz provided from the CPU card is input to the DSP (IC109 - 53pin) as a basic clock.
This clock is input to the PLL inside DSP. PLL generates 14.336MHz(PLLCLK) from this clock. PLLCLK is divided into four inside and generates CLKOUT1 and CLKOUT2.
Figure 4 - 22 is standing of CLKOUT1 and indicates the third phase (Q3) is about to begin. Hereafter, phase no. Q1 - Q4 explains the bus operation.

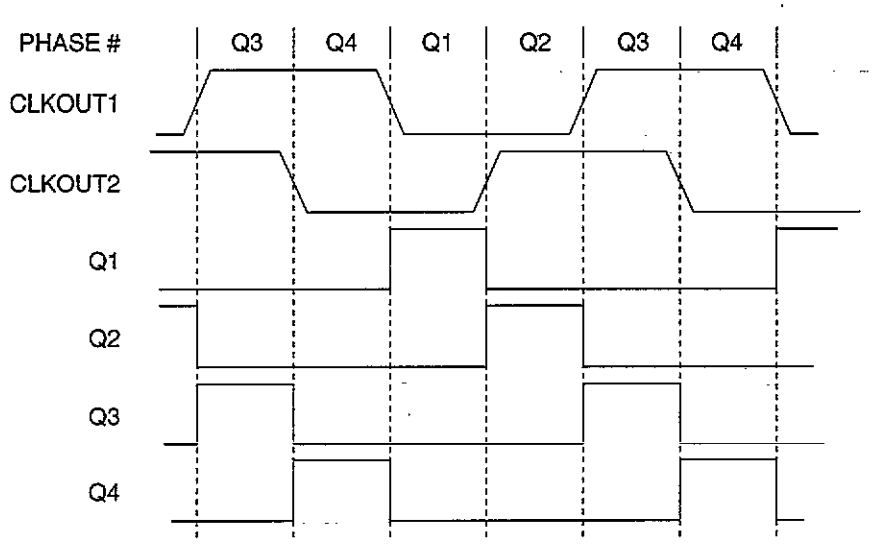


Fig. 4-24. DSP Clock

2-4. Parallel DSP Port

DSP installs control signals mentioned below to interface with Program ROM or a IC101 inside register.
- •16bit parallel data bus (A15 - A0)
- •16bit parallel data bus (D15 - D0)
- •Chip select (PS, DS)
- •Timing Control (STRB, R/WN)

(1) External read out cycle

The following are phenomena generated with the external read out cycle.

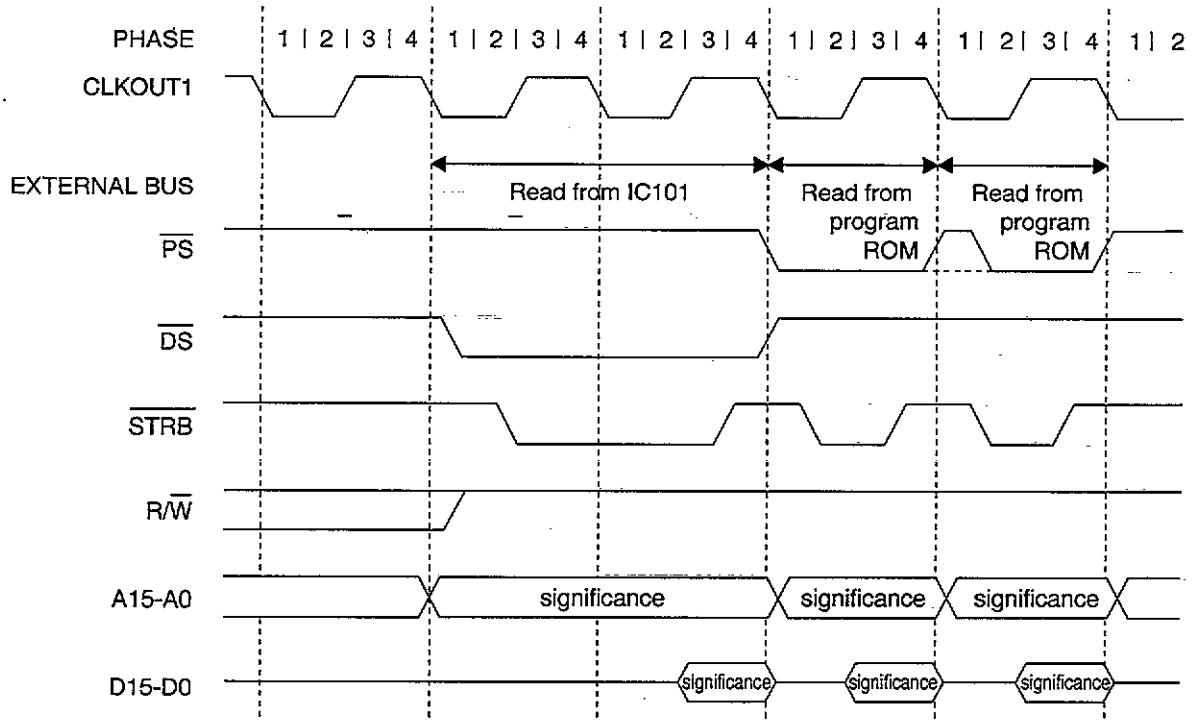
1) In the first phase (Q1), DSP starts driving address bus, and makes either PS or DS low level. To indicate the external memory's read out, R/W signal becomes high level.

2) At the beginning of the second phase (Q2), STRB signals indicating the effectiveness of the address bus output, and is used to generate a read enable signal with the R/W signal.

3) At the end of the third phase (Q3), data is taken in.

4) At the beginning of the fourth phase (Q4), the STRB signal is cancelled. PS, or DS signal and address bus are of no effect, and ends the external read out cycle.

Control signal PS, DS, STRB and R/W are generated only when the external memory location has gained access to. PS is asserted only when Program ROM (IC107/IC108) has gained access . DS is asserted only when the internal register of IC101 has gained access.



Timing 4-22. Read Cycle

(2) External write in cycle

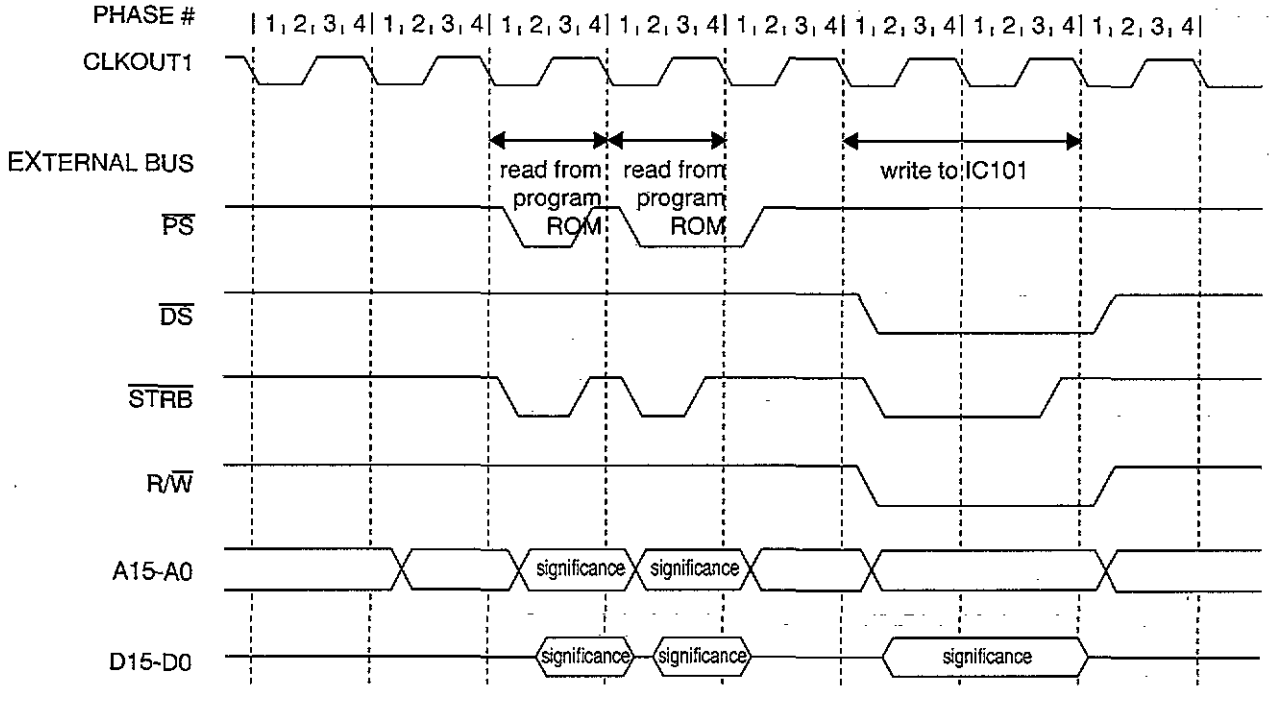
The following are phenomena generated with the external write in cycle.

1) In the first phase (Q1), DSP starts driving address bus, and makes DS active low. The R/W signal be comes low level for writing in external memory .

2) At the beginning of the second phase (Q2), the STRB signal indicates the effectiveness of the address bus output, and is used to generate read a enable signal with the R/W signal.

3) At the beginning of the second phase (Q3), data bus becomes active.

4) At the beginning of the fourth phase (Q4), the STRB signal is canceled. The Processor makes the address bus and DS signal invalid, and ends access of the external write in cycle.

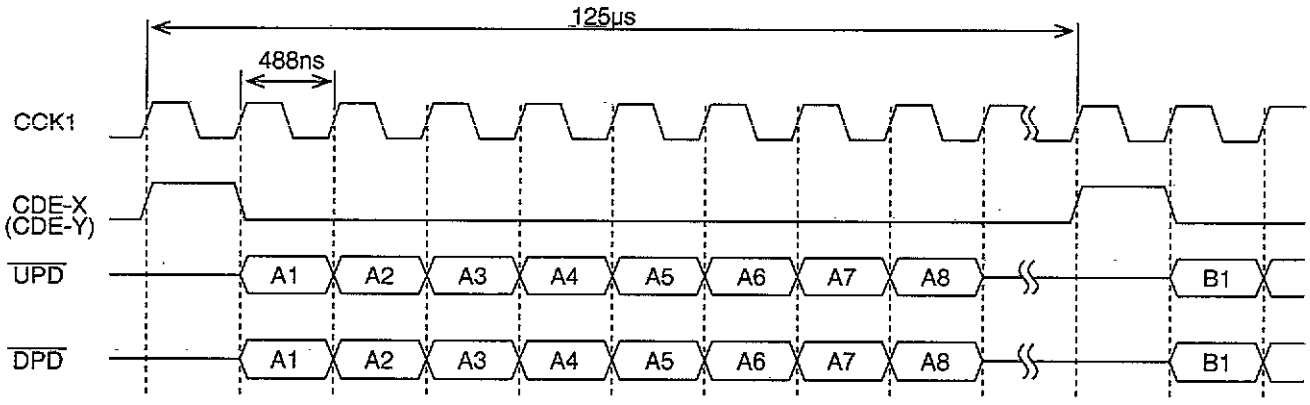


Timing 4-23. Write Cycle

2-5. DSP serial port

DSP serial port is used with the interface for the D-PITS B channel (Digital Voice Data).
This port is connects IC101 with CCK1, UPD, DPD, CDE-X(IC109A) and CDE-Y(IC109B) signals.
CCK1 is a 2.048MHz's serial shift in/out clock. UPD is 8bit PCM formatted voice data output from DSP. It is sent out to the PBX through D-PITS interface logic internal IC101. DPD is DSP input of PCM formatted voice data received from the PBX. CDE-X(CDE-Y) is an 8 KHz frame pulse input to enable to send or receive effective data of a serial port.

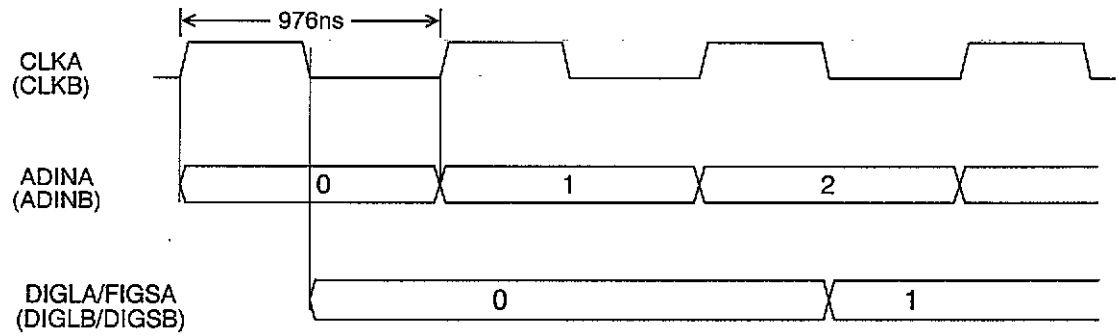
Serial Port Transfer Timing is shown in Timing 4-24.



Timing 4-24. DSP Serial Port

2-6. DSP Codec Port

The DSP Codec Port is input and output from a Single line telephone interface. It is used for interface with a codec converting analog voice data to digital data. DSP uses four interface lines (CLK, ADIN, DIGS and DIGL), then communicates Codec. These signals are connected with Codec (IC 241) on a COL card through CN102.
1.024MHz's CLKA (CLKB) output from the DSP is used as a sampling clock for DAC/ADC internal codec.
ADIN is a serial voice data input to DSP. (Bit rate = 1.024MHz) DIGLA/DIGSA (DIGLB/DIGSB) is 2 bit voice data output from DSP. (Bit rate = 512 KHz)
Input and output timing of Codec Port is shown in Timing 4 - 25.



Timing 4-25. DSP Codec Port

2-7. CO line control port

A CO line control port is provided by IC 101. Microprocessor, by programming COL Control register inside IC101, controls ON/OFF by a single line unit. This port is connected to the COL card through CN 102. This Port includes the mentioned CO line Control functions.

Function	CN102 pin No.	Description
BELL Detection	9 (BELLA) 5 (BELLB)	These Signals respond to the ring signal from the single line telephone interface.
CPC Detection	7 (CDETA) 3 (CDETB)	These signals indicate temporary disconnection of the single line telephone interface.
Hook Control	12 (PULSA) 8 (PULSB)	These signals control the Hook condition of the single line telephone interface. If it is low, the telephone line is in the OFF-Hook condition. If it is High, it is in the ON-Hook condition.
Loop Back Control	11 (LOOP)	This signal allows loop back testing of the analog voice data for diagnostic. If it is low, it is in test mode. In normal operation, LOOP is held in High.
Reserved	10 (RURSA) 6 (RURSB)	These signals are not used.

2-8. D-PITS digital interface

D-PITS digital interface is provided with IC101. D-PITS interface built-in IC101 extracts effective data (2B + D) from a receiving D-PITS data stream, transfers D channel receiving data to voice port, and B channel receiving data (PCM Voice Data) to DSP. Sending out D-PITS data stream formed with D channel sending out data received from Voice Port and B channel sending out data received from DSP, is output to the COL card. D-PITS interface is a digital interface, line bit rate : 512kBPS's, 2 line time share data format. Its communication format is 2B+D (B:64kBPS, D:16kBPS) and executes ping-pong communication every 8kHz (125us).

Data format B channel is 64kBPS u/A PCM format and D channel is 16kBPS HDLC format.

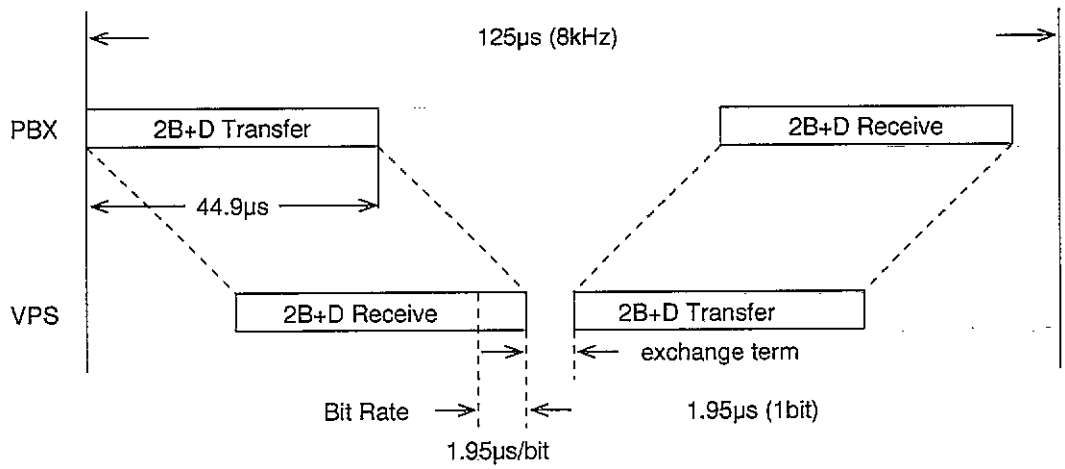


Fig. 4-25. D-PITS Data Transfer

Bit allotment of the DPITS frame is described below. S(1 - 5) is a zero pattern of 5 bits and is used as hardware to synchronize receiving and sending data with PLL.MA (1 - 3) is a 3-bit zero pattern data against AM1 symbolization and is used to detect the head of effective data. HK sends out an installed value inside the HK port. D(0 - 1) is 2 bit/frame HDLC data channel. B1 (7 - 0), B2 (7 - 0) are received and sent out in an 8-bit PCM data by MSB first individually.

S	S	S	S	S	M	M	M	H	D	D	B	B	B	B	B	B	B	B	B	B	B	B	B	B	P
1	2	3	4	5	A	A	A	K	0	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	R
					1	2	3				7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Y
5					3				2		8								8							1	

Fig. 4-26. D-PITS Frame Format

3. COL CARD

3-1. Overview of the COL CARD

Function block diagram of the COL Card is shown in figure 4 - 27.

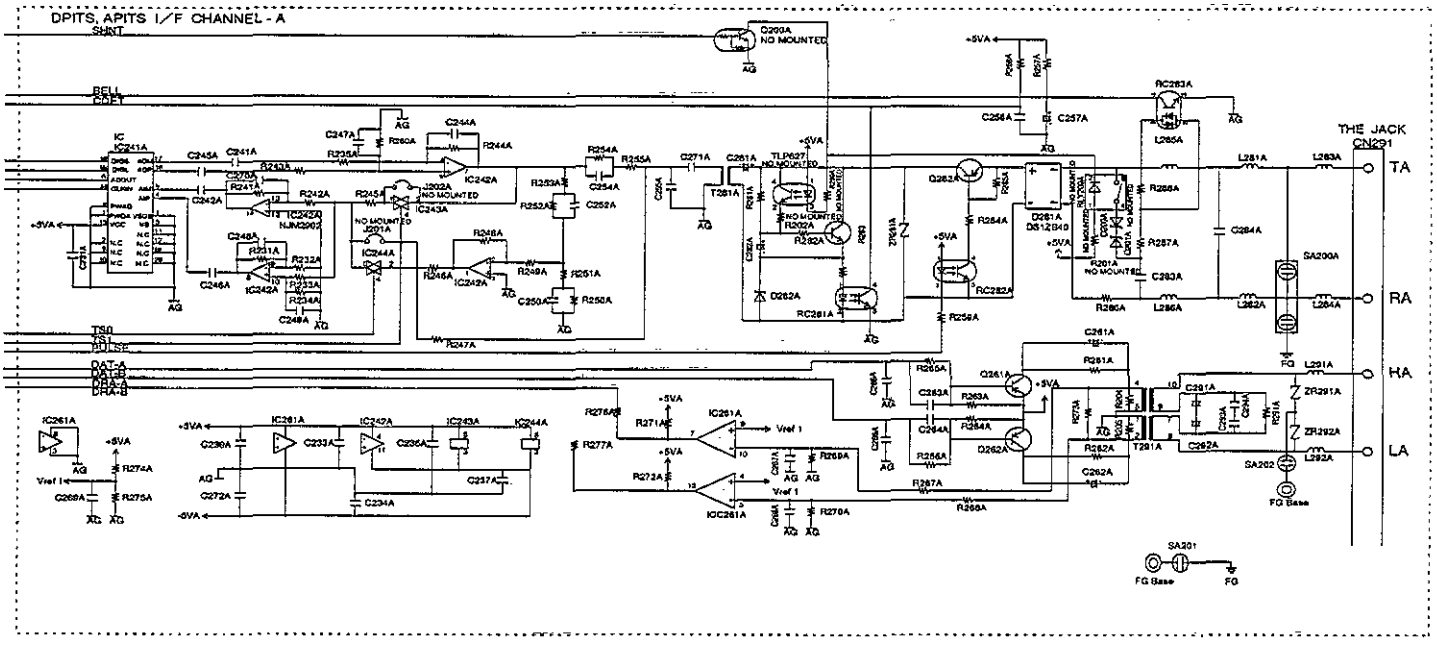


Fig. 4-27. Functional Block Diagram of COL Card

The COL Card possesses 2 channels, SLT (Single line Telephone) interface and 1 channel D-PITS line interface.

The SLT interface includes Codec, Amplifier, 4W - 2W Converter, Transformer CPC Detector, Hook Control, Bridge and Bell detector.

The D-PITS interface includes Receiver, Transceiver and Transformer.

3-2. CODEC (IC241)

The Codec provides a voice-band ADC and DAC. The Codec communicates with the DSP using a 4 interface line (DIGS, DIGL, ADOUT and CLKIN). The DAC logic can synchronously operate in full duplex with ADC.

Figure 4 - 28 shows the internal function block.

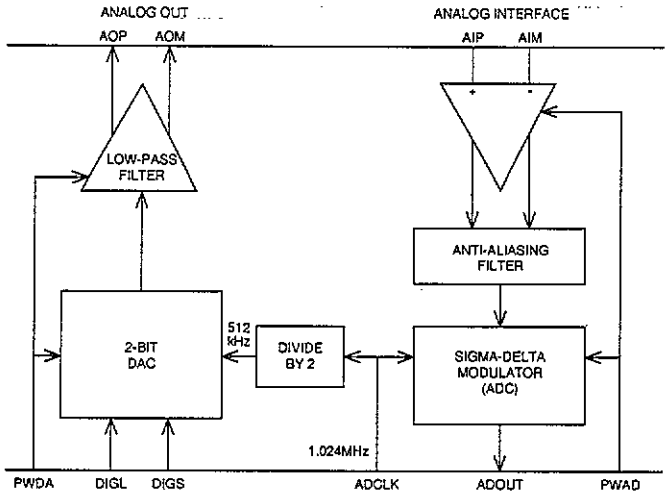


Fig. 4-28. Codec Internal Block Diagram

3-3. Amplifier (IC242)

This logic amplifies the voice band analog level.

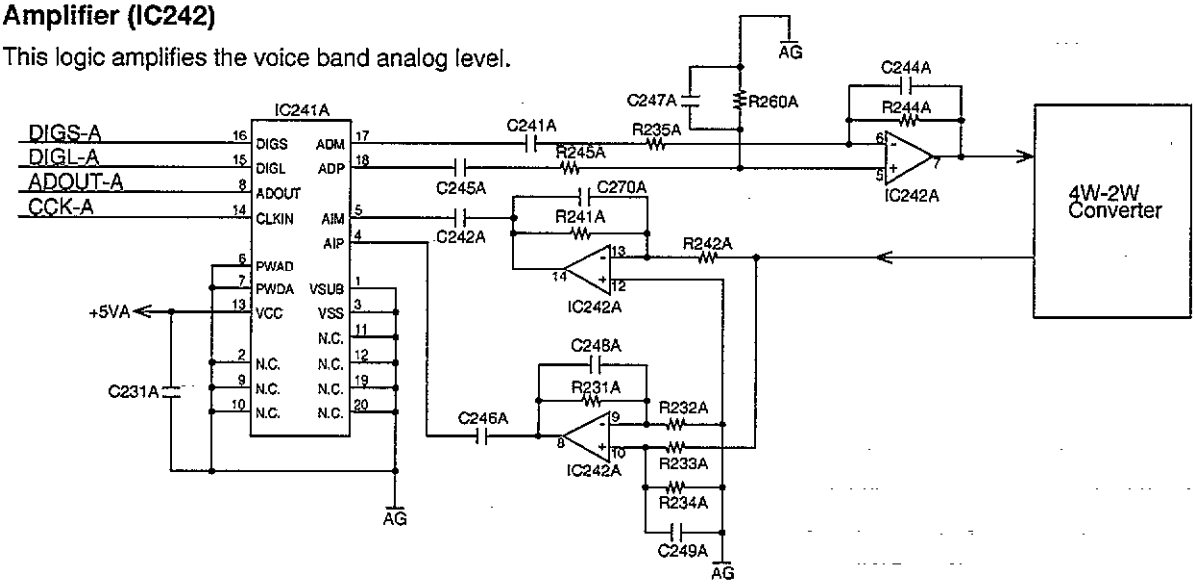


Fig. 4-29. Amplifier Logic

The data flow is shown as follows.

•Transmit Voice Data

IC241 - 17 (ADM out) → C241 → R235 → IC242 - 6 → IC242 - 7 → 4w - 2w Converter.

IC241 - 18 (ADP out) → C245 → R243 → IC242 - 5

•Receive Voice Data

4w - 2w Converter → R242 → IC242 - 13 → IC242 - 14 → C242 → IC241 - 5 (AIMin)

→ R233 → IC242 - 10 → IC242 - 8 → C246 → IC241 - 4 (AIPin)

3-4. 4W - 2W Converter

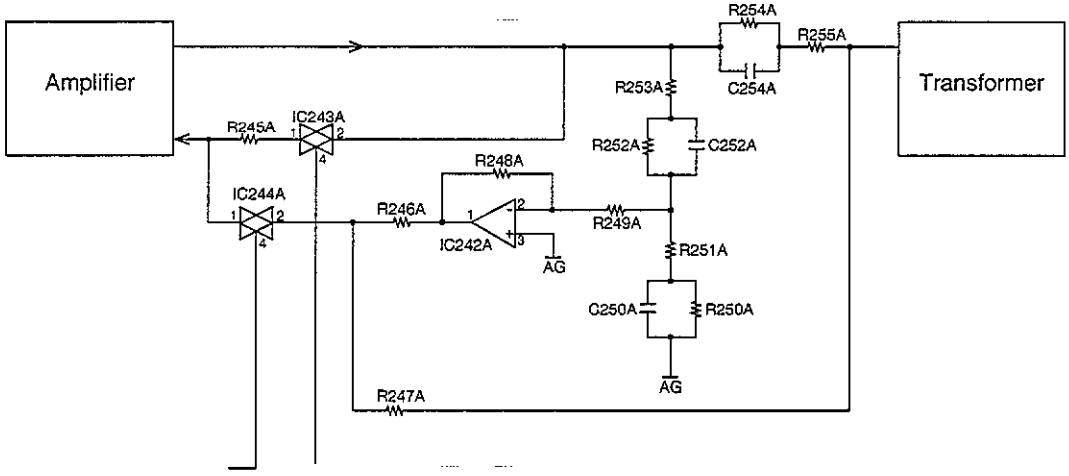


Fig. 4-30. 4W-2W Converter Logic

This logic converts a 4 line analog signal to a 2 line analog signal.
The data flow is as follows.
•Transmit Voice data
Amplifier → R254 → R255 → Transformer (Transmit data)
R253 → R252 → R249 → IC242 → R246
•Receive Voice Data
Transformer → R247A → IC244 - 2 → IC244 - 1 → Amplifier

3-5. CPC Detector

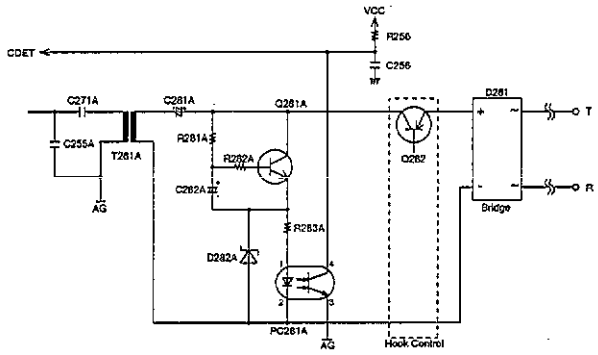
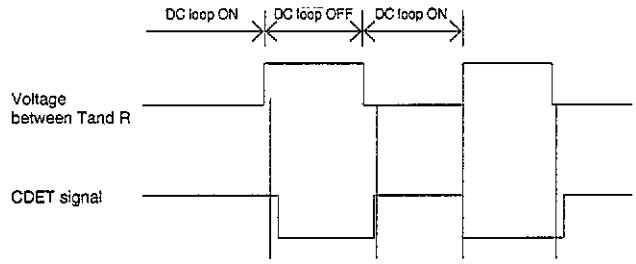


Fig. 4-31. CPC Detector

This logic detects temporary disconnection of the DC loop current on the telephone line at off hook condition. The DC loop current flows through T → D281 → Q282 → Q281 → R283 → PC281 - 1 → PC281 - 2 → D281 → R. When DC loop is ON, photocoupler PC281 pin 4 - 3 is OFF and CDET signal drives to high. When DC loop is OFF, photocoupler PC281 pin 4 - 3 is on and CDET signal drives to low.



Timing 4-26. CPC Detector

3-6. Hook Control

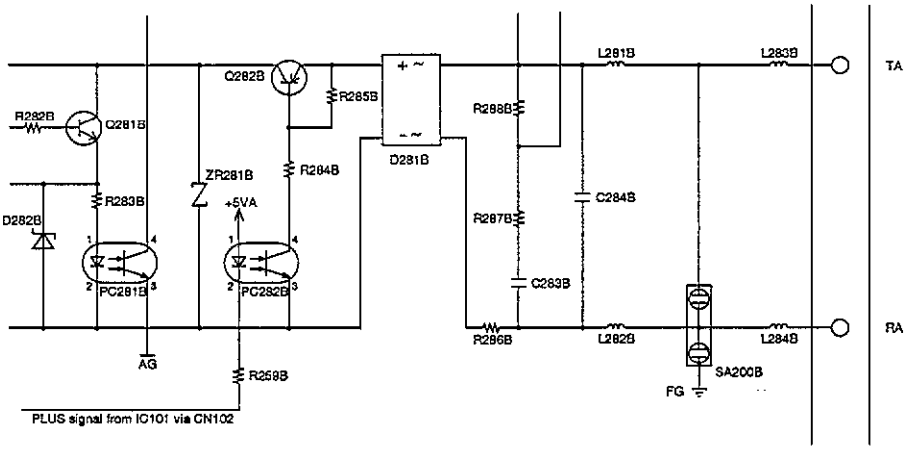


Fig. 4-32. Hook Control

This logic controls the DC loop ON/OFF of the SLT interface. When at the ON hook condition, a PLUS signal is driven to High Level by the Co line control Port on IC101. In this condition, photocoupler PC282 pin 4 - 3 is ON and Q282 is turned OFF. When at the OFF Hook condition, a PLUS signal is driven to low level and Q282 is turned on. As a result, the DC current flows through the following path.

DC loop path: A → L283 → L281 → L285 → D281 → Q282 → Q281 → R283 → PC281 → D281 → R286 → L286 → L282 → L284 → B

3-7. Bell Detector

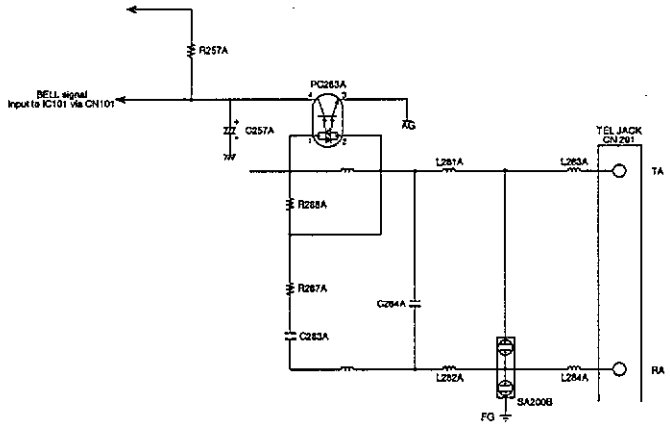
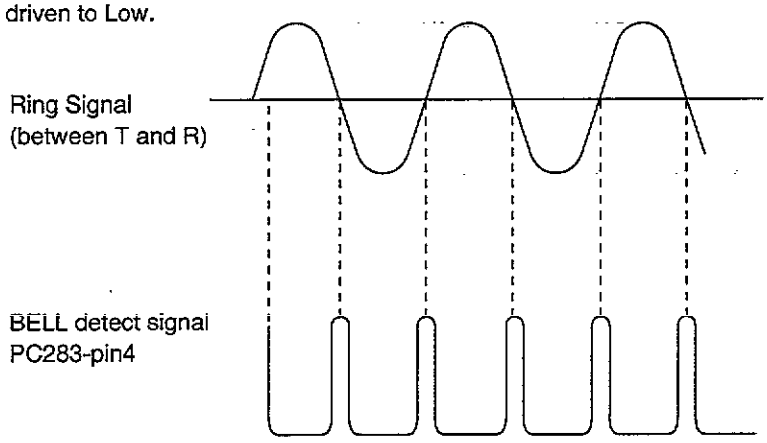


Fig. 4-33. Bell Detector

This logic detects the ringing status input from the SLT line at the ON Hook Condition. The ring signal flows through A → L283 → L281 → L285 → PC283 → R287 → C283 → L286 → L282 → L284 → B.

If the ringing signal level over the threshold level of the PC281, photocoupler PC283 pin 4 - 3 turn to ON. In this case, the Bell signal is driven to Low.



Timing 4-27. Bell Detector

3-8. D-PITS Line Receiver

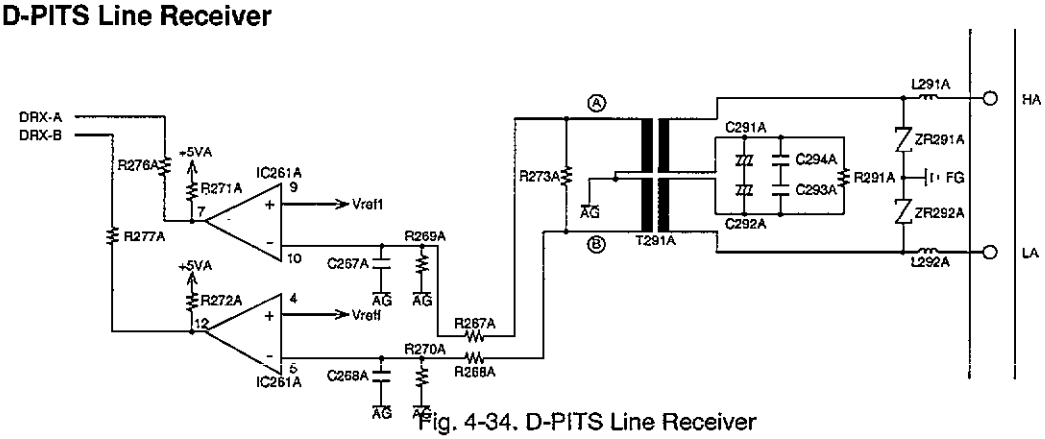


Fig. 4-34. D-PITS Line Receiver

This logic allows the D-PITS to receive reception data from the PBX. R291A

The D-PITS reception data flows through HA → L291A → T291A (8 - 7) → C291A → C292A → T291A (6 - 5) → L292A.

3-9. D-PITS Line Transceiver

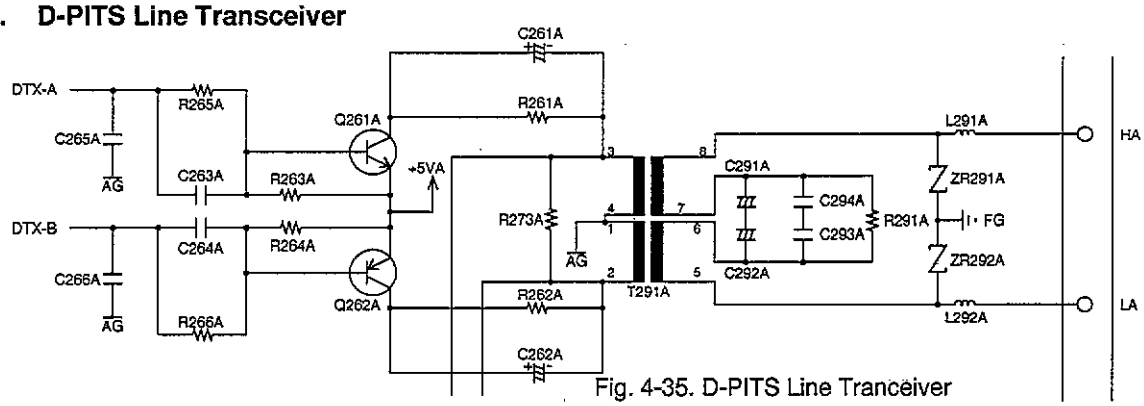


Fig. 4-35. D-PITS Line Tranceiver

This logic allows the D-PITS to transmit transmission data to the PBX.

The D-PITS transmission signals flow as follows.

R265A

DTX - A = IC101 - 17 → R113 → CN102 - 28 → C263A → Base of Q261A.

DTX - B = IC101 - 18 → R114 → CN102 - 29 → R266A → Base of Q262A.

C264A

If IC101 drives DTX - A (DTX - B) to low level, Q261A (Q262A) is turned ON and the loop current flows through as follows.

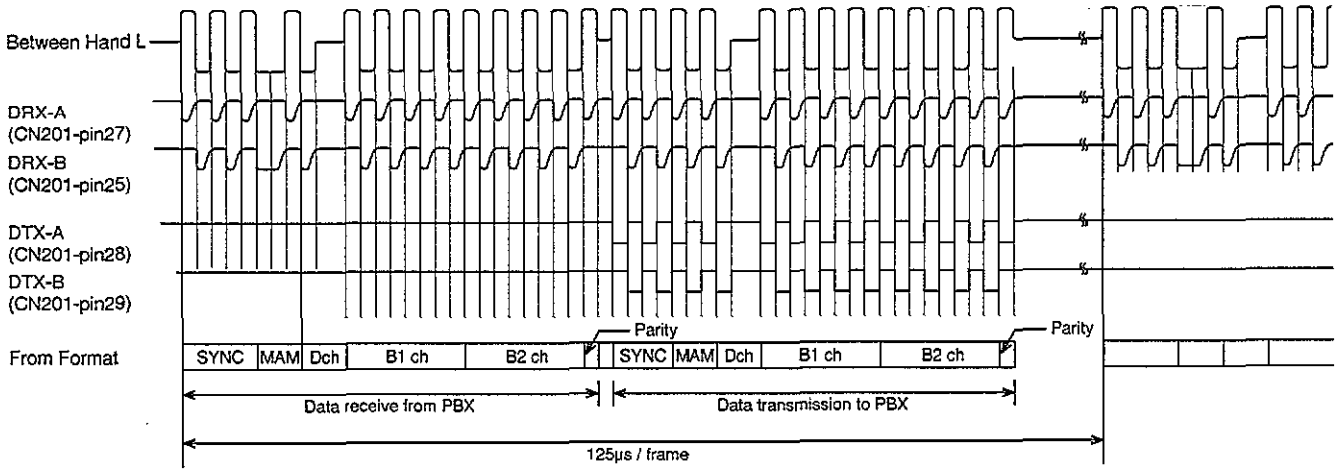
R261A

+5VA → Q261A (C - E) → C261A → T291A (3 - 4) → AG

+5VA → Q262A (C - E) → R261A → T291A (2 - 1) → AG

C262A

This loop current transition generates the D-PITS transmission data between T291A - pin 8 and T291A - pin 5. As a result, T291A drives the HA - LA line corresponding with DTX-A/DTX-B.



Timing 4-28. D-PITS Transmission

UTILITY COMMANDS

In this chapter, we explain commands which can be used by a general user.
In order to use, choose <Utility Command> in <System Administration Top Menu> of Administrator Service.
Command waiting prompt is on the screen. (See below.)

```
$
```

Input command after "$".

```
$ command
```

1. HELP COMMAND (HELP)

(1) Function

To show the list which can be used in the VPS.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$HELP
    ONLN            : System Online
    OFLN            : System Offline
    PASS            : Password setting
    TIME            : Time & Date setting
    PSET            : Report Print Out Time setting
    ELOG            : Device Error Log Listing
    SAVE            : VPS Program & Data Save (VPS -> PC : Xmodem)
    LOAD            : VPS Program & Data Load (VPS <- PC : Xmodem)
    GPRN            : Parameter Global Printing
                      ( only 'ASCII Terminal' mode )
    VERS            : Program Version Check
    QSET            : Quick Setup
    MWL             : MWL Retry count Set (1-3)
    MRL             : Minimum Recording Length Set (0-3)
    MPLT [opt]      : Registered User Prompt No. List
                      [opt] : 1     -->  User Prompt 1
                              2     -->  User Prompt 2
                              None  -->  User Prompt 1&2
    CREP [no]       : Custom Menu Information List
                      [no]  : Custom Menu No. (1-100)
    CCLR [no]       : Custom Menu Access Counter Clear
                      [no]  : Custom Menu No. (1-100/0) (0:Clear All)

    (the following are displayed only for privileged managers)

    DCLR [drv], [opt] : Initialize parameters and Data
                        [drv]  1 or 2
                        [opt]  0 : All Parameters and Voice Data
                               3 : All Parameters and Voice Data
                                   except Usr Prompts
                               4 : Only Usr Prompts
    DCPY            : Disk      Copy DISK1  =>  DISK2
    PCPY            : Program   Copy DISK1  =>  DISK2
    GCPY            : Guidance  Copy DISK1  =>  DISK2
    XCPY [opt]      : Program, System Guidance Copy DISK2  =>  DISK1
                      [opt]  None  : Program & System guidance
                             1     : Program
                             2     : System Guidance
                             3     : User Prompts
    SYSD            : System Disk Set Up (DISK2)
    LMON            : Line Monitor
```

2. ONLN Command (on line service control)

(1) Function

VPS service is resumed.

Please refer to < 1.2 OFLN command> for OFLN command.

(2) Operand

Nothing.

(3) How to use, example for usage

a) When throwing normal on line command

```
$ONLN
 **    ON LINE MODE   **
```

b) Below mentioned cases don't become on line condition.

- In the D-PITS interface, D-PITS communication circuit is not connected. Or Communication circuit connected the install on PBX side is not shared as VM port in DPITS interface.
- There is no DSP/CO card.

```
$ONLN
 **    OFF LINE MODE   **
```

3. OFLN COMMAND

(1) Function

To break VPS service.

VPS service is suspended.

(2) Operand

Nothing.

(3) How to use, example for usage

a) When throwing command, VPS service is not used.

```
$OFLN
 **    OFF LINE MODE   **
```

→ Becomes off line service immediately.

b) When throwing command, VPS service is used.

```
$OFLN
 ***    Now Line is used !!   *** <WAIT>
```

→ The execution of this command is in the waiting condition, when service usage finishes, the command is executed.

```
** OFF LINE MODE **
```

4. PASS COMMAND (Install password)

(1) Function

To install and cancel administrator and system passwords.

An Administrator password is the password to enter from the initial screen to the terminal select screen.

A System reset/clear password is the password to be asked when reset is executing on the <System Reset/Clear> screen.

Without a password, installation is possible in both cases.

The Password should be one word with less than 8 letters or numbers, or special symbols (underline, period, space).

(2) Operand

Nothing.

(3) How to use, example for usage

```
$PASS
 1 : Administrator Password  2 : System Reset/Clear Password : =
```

① In the of case new registration

Select 1 or 2.

```
$NEW PASSWORD : =
```

Input password.

```
$VERIFICATION : =
```

To confirm password, input password again.
When it is different from the first one, start from <New Password> again.

Note: Input password is not shown on the screen.

② Change

Select 1 or 2.

```
$OLD PASSWORD : =
```

Input present registered password.

```
$NEW PASSWORD : =
```

Input new password.

```
$VERIFICATION : =
```

To confirm input password, input the password again.

Note: When it is an administrator password, <present password> is not required.

③ Password cancellation

Select 1 or 2.

```
$OLD PASSWORD : =
```

Input present registered password.

```
$NEW PASSWORD : =
```

Press return key without inputting anything.

```
$VERIFICATION : =
```

Press return key without inputting anything.

5. TIME COMMAND (Installation of Time/Date)

(1) Function

To install time and date.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$TIME
  Current time is 12 : 34, PM
  Enter new time  ( hh : mm, AM/PM ) : =
```

Input current time.

Example: In the case of 2:56 PM.

Enter new time (hh:mm, AM/PM) : = 2:56, PM

```
Current date is 29-JAN-'93
Enter new date  ( DD-MM-YY ) : =
```

Input current date (Date - Month - Year) (Input last two figures for year)

example: In the case of July 13th. 1973

Enter new date (DD - MM - YY) : = 13-7-73

Note: Input time and date correctly, because VPS service owes much of its work to time and date. Following are also changed with the change of time and date.
Notification of arrival, Message auto distribution send, Designated time between mail boxes message distribution send, Auto transfer function, etc.

6. PSET COMMAND (Install report printing out time)

(1) Function

This command makes it possible to print out reports at a certain time.

The Following reports are printed out.

① Disk Usage Report

② Port Usage Report

③ Call Account data Report

(2) Operand

Nothing.

(3) How to use, example for usage

```
$PSET
  Report Print Out Service  [ Disable ]
    1 : Enable   2 : Disable : =
```

Input 1 for install, input 2 for cancellation.

When you input 1, still more install the time for printing out.

```
Enter The Print Out Time  ( hh : mm, AM/PM ) : =
```

Example: In the case of 2:56 PM

Enter the Print Out Time (hh:mm, AM/PM) : = 2:56, PM

7. ELOG COMMAND (Display device error)

(1) Function

To display the error trace of the DSP card, MAIN card, Hard disk, etc.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$ELOG
        DEVICE          ERROR                   TIME
        ------          -----                   ----
 1.     CPU             MEM-GET                 14-JUL 14:00 PM
 2.     CLOCK                                   15-JUL 12:40 AM
 3.     DISK            DATA R/W (xx/yyyy)      15-JUL 13:02 PM
 4.     DSP1            SCAN                    15-JUL 13:02 PM
 5.     DSP4            FIFO                    15-JUL 13:15 PM
 6.     CPU             APPLICATION (2)         15-JUL 13:16 PM
```

[Explanation]

• The following examples of errors.

CPU	MEM - GET	CPU card impossible to acquire memory.
	APPLICATION (n)	Application error occurred momentarily while working.
CLOCK		Hindrance occurred in clock IC.
DISK	DATA R/W (XX:YYYY)	R/W error in hard disk. (master) XX : error code YY : error sector No.
DSPn	SCAN	DSP Card n is not equipped. CPU cannot confirm the DSP card.
	FIFO	DSP or FIFO error occurred momentarily while working.

Note: n Card No. 1 ~ 4

• After displaying the error contents, it asks whether to clear the error trace data or not.

```
Clear ? ( Y/N ) : =
```

You can clear the error trace data by inputting "Y".

8. SAVE COMMAND (Program/Data Back up)

(1) Function

To back up a certain program or data on the VPS hard disk.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$SAVE
      Disk Data Down-load  ( Xmodem )
            1 :  Program
            2 :  Parameters
            3 :  System Prompts
            4 :  User Prompts-1
            5 :  User Prompts-2
            6 :  Custom Service Menu
            7 :  Personal Greeting
 Select No. : =
```

Select the item to be backed up.

```
To start press 'RETURN'
```

Press the return key.

```
Start _ _ _ _ _ Download !!
```

To select the data receiving mode (Xmodem) in DTP, point to the name of the file to be backed up. Now it is possible to transfer the data by Xmodem protocol.

Note:

① Command cancellation before transfer → '¥' or '＼'

② Transfer cancellation during receiving → follow your communication software.

Note: Please refer to another sheet for the details of SAVE command.

9. LOAD COMMAND (Program/Data up-date)

(1) Function

To update a certain program or data on the VPS hard disk.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$LOAD
      Disk Data Up-load ( Xmodem )
            1 : Program
            2 : Parameters
            3 : System Prompts
            4 : User Prompts-1
            5 : User Prompts-2
            6 : Custom Service Menu
            7 : Personal Greeting
 Select No. : =
```

Select the item to update.

```
To start press 'RETURN'
```

Press the return key.

```
Start _ _ _ _ _ Upload !!
```

To select the data receiving mode (Xmodem) in DTP, point to the name of the file for update. Now it is possible to transfer data by Xmodem protocol.

Note:

① Command cancellation before transfer → '¥' or '\'

② Transfer cancellation during receiving → follow your communication soft.

Note: Please refer to another sheet for the details of LOAD command.

10. VERS COMMAND (To display each card and program version of hard disk)

(1) Function

To display CPU ROM and the program version on the hard disk.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$VERS

 V.P.S. PROGRAM VERSION

   MAIN DISK  : V10100 (1.03) ..... ①
   MAIN ROM   : V011B  (1.03) ..... ②
```

[Explanation]

①Hard disk • program version display

MAIN DISK : Version (Internal version)

Note: Users do not need to pay attention to <Internal version>.

②CPU ROM • program version display

MAIN ROM : Version (Internal version)

11. QSET COMMAND (Quick Setup)

(1) Function

To start Quick Setup.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$QSET

Thereafter, Quick Setup Menu starts.
```

12. MWL COMMAND (To install the number of Message Waiting lamp retry)

(1) Function

In case the message waiting lamp turn fails to on and off, VPS retries after a certain period.
With this command the number of retries can be installed.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$MWL
  Current Setting of M.W.L. Retry Count is 3
  Enter M.W.L. Retry Count (1-3) : =
```

→ Select the number of retry (1 ~ 3 times)

13. MRL COMMAND (To install the minimum time of message recording)

(1) Function

With this command, the minimum time of message recording can be installed. A message shorter than installed here doesn't seem to be a message, so not be recorded.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$MWL
  Current Setting of Minimum Recording length is 3
  Enter Minimum Recording length (0-3) : =
```

→ Input the recording time by seconds (range: 0 ~ 3 seconds)
To input 0 seconds means all recorded messages are effective.

14. MPLT COMMAND (Display registered user prompt)

(1) Function

To display prompt No. of registered (recorded) user prompt

(2) Operand

Nothing.

$MPLT

(3) How to use, example for usage

```
$MPLT
***** List of Registered User Prompt 1 No. ( [1], [2], . . . , [619] ) *****

  1,   2,   3,   4,   5,   6,   7,   8,   9,  10,  11,  12,  13, ...
 21,  22,  23,  24,  25,  26,  27,  28,  29,  30,  31,  32,  33, ...
 41,  42,  43,  44,  45,  46,  47,  48,  49,  50,  51,  52,  53, ...
 61,  62,  63,  64,  65,  66,  67,  68,  69,  70,  71,  72,  73, ...
 81,  82,  83,  84,  85,  86,  87,  88,  89,  90,  91,  92,  93, ...
101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, ...
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...

Total Number Registered = 419                              ..... ①

***** List of Registered User Prompt 2 No. ( [1], [2], . . . , [619] ) *****

  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  .   .   .   .   .   .   .   .   .   .   .   .   .   .   .
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...
  ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   ,   , ...

Total Number Registered = 0                                ..... ②
```

[Explanation]

① The total number of registered User Prompt 1.

② The total number of registered User Prompt 2.

15. CREP COMMAND (Display custom menu information)

(1) Function

To display installed information inside the designated number' custom menu.

In case the custom menu is nested, it is displayed in stages (maximum of 8).

(2) Operand

It is possible to select from 1 to 100 with the custom menu number display.

(3) How to use, example for usage

```
$ crep 20
Custom  [ 20]   ( User-1 ) ( Access :   0 ) ( Menu Msg. : None )
                    ↓           ↓          ↓          ↓
          (Remarks 1)  (Remarks 2)  (Remarks 3)  (Remarks 4)
 |  < Custom Service Entry Menu > → (Remarks 5)

[1]-Xfer Mbx (401)          → (Remarks 6)

[2]-Xfer Extn (402)         → (Remarks 7)

[3]-Custom [ 21] (System) (Access :   0) (Menu Msg. : None)
 |      |  < Voice Mail Information Eng. >
 |     [1] – Custom [ 22] (User-2) (Access :   0) (Menu Msg. : None)
 |      |      |  < Voice Mail Information Eng. >
 |      |      [1]- Operator
 |      |      [2]- Name Dial
 |      |      [3]- Subscriber
 |      |      [4]- Dprt Dial
 |      |      [*]- Main Menu
 |     [*]-Main Menu
[6]- Operator
[7]- Exit
[8]- Pre. Menu
[*]- Main Menu
[#]- Exit
$
```

Note:

Remarks 1) Custom menu No.

Remarks 2) Prompt kind (System / Use - 1 / User - 2)

Remarks 3) Custom service access number

(How many times this custom menu is accessed by telephone service.)

Remarks 4) The condition of menu message recording (Rec / None)

Remarks 5) Description

Remarks 6) Mail box number

Remarks 7) Extension number

16. CCLR COMMAND (To clear custom menu access number)

(1) Function

To clear a selected number of custom menu access number.(The number of times custom service number was accessed by telephone service.)

(2) Operand

It is possible to select from 1 to 100 with the custom menu number to clear.
When 0 is selected, all of the custom menu is cleared.

(3) How to use, example for usage

```
$ CCLR 20
  Custom Menu < 20 > Accessing Counter is Cleared

$ CCLR 0
  All Custom Menu Accessing Counters are Cleared
```

17. DCLR COMMAND (Initialize parameter, data of hard disk)

(1) Function

To clear the parameter or data of the selected drive's hard disk.
The following is to be cleared.

- Each parameter (Mail box information, report information, etc.)
- Voice data (system guidance, user guidance, message, etc.)

After execution, VPS should start up again.

(2) Operand

```
$DCLR [drv] [opt]
```

① [drv]
Select drive No.
1 : Drive 1
2 : Drive 2

② [opt] (Option)
Select the parameter and data to be cleared.
0 : Install hard disk to system disk, then clear all parameters and voice data.
1 : Install hard disk to option disk, then clear all voice data.
3 : Install hard disk to system disk, then all parameters and voice data, except for user guidance.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) ①
4 : Clear user guide only.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) ①

(3) How to use, example for usage

Example is shown blow.

```
$DCLR 1,0                    ..... ①
  Please POWER OFF !         ..... ②
$DCLR 2,3                    ..... ③
  Please POWER OFF !
$DCLR 1,4                    ..... ④
  Please POWER OFF !
```

[Explanation]

①To clear all parameters and voice data in drive 1.

②To display the message urges to start up VPS again.

It won't accept key input at all. Turn the power off and then on.

③To clear all voice data except user prompt in drive 2.

④To clear all user prompts in drive 1 and user prompt 2.

18. DCPY COMMAND (All selector copies between drives)

(1) Function

To copy the data (all sector) in drive No. 1 to drive No. 2.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$DCPY
  001234                     ..... ①
$                            ..... ②
```

[Explanation]

①To display the sector number of present copying.

②To display command prompt "$".

It means copy finishes normally.

Note:

When an error caused by the hard disk occurs during execution of DCPY, the error sector number is displayed. The sector is skipped, then disposition continues. It is recommended to check the sector with the RECO command and execute recover after DCPY finishes. Concerning the RECO command, please refer to <Chapter 8 8.7 RECO command>.

The following are the commands displayed during error sector copying.

- DCPY
- PCPY
- GCPY
- XCPY
- SYSD

19. PCPY COMMAND (Program copy between drives)

(1) Function

To copy the VPS program in drive No.1 to the program region of drive No.2.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$PCPY
 001234 ..... ①
$       ..... ②
```

[Explanation]

①Sector number presently copying.

②To display Command prompt "$".

20. GCPY COMMAND (System guidance copy between drives)

(1) Function

To copy system guidance in drive No.1 to drive No.2.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$GCPY
 001234 ..... ①
$       ..... ②
```

[Explanation]

①Sector number under presently copying.

②To display Command prompt "$".

21. XCPY COMMAND (Copy from drive No. 2 to drive No. 1)

(1) Function

To copy from drive No.2 to drive No. 1. The following are copy objects.

①Program

②System guidance

③User prompt

(2) Operand

```
$XCPY [para]
```

①[para]

Nothing	: Program, System guidance copy	(Drive 2 → Drive 1)
1	: Program copy	(Drive 2 → Drive 1)
2	: Program copy	(Drive 2 → Drive 1)
3	: Program copy	(Drive 2 → Drive 1)

(3) How to use, example for usage

```
$XCPY                                                    ..... ①
 001234                                                  ..... ②
$                                                        ..... ③
$XCPY 3                                                  ..... ④
 XCPY (User-Prompt Copy Disk2 -> Disk1)  Start !         ..... ⑤
 001234
 XCPY (User-Prompt Copy Disk2 -> Disk1)  End !           ..... ⑥
  *** Total Copy Number : 125***                         ..... ⑦
$
```

[Explanation]

①To copy program and system guidance.
②To display sector number presently copying.
③To display command prompt "$".
Copy ends normally.
④To copy user prompt.
⑤To display copy starts.
⑥To display copy ends.
⑦To display the user prompt's total number copies.

22. SYSD COMMAND (Install Drive 2 to system disk)

(1) Function

The Following jobs are required to install Drive No.2 to a system disk.
①To initialize Drive 2. (FORMAT 2)
②To clear Drive 2. (DCLR 2, 0)
③To copy program from Drive 1 to Drive 2.
To copy system guidance from Drive 1 to Drive 2.
To copy user prompt from Drive 1 to Drive 2.
During this operation you can choose to copy-only user prompt 1 or only user prompt 2 or both user prompt 1 and 2. (To put coming up prompt No. in order, then store in Drive 2.)

(2) Operand

Nothing.

(3) How to use, example for usage

```
$SYSD
 Select User Prompt No.  ( 0-2, 9 )
  Ex.     If you select No. 1,

          Only User Prompt 1 is copied from Disk1 to Disk2.

             0 :  User-1 & User-2
             1 :  User-1
             2 :  User-2
             9 :  Not Copy User Prompt  = => 2

 *** FORMAT  ***                                         ..... ①
 *** DCLR    ***                                         ..... ②
  ****************
 *** COPY   ***                                          ..... ③
    0005A0
    0020a0
 *** USRP COPY* * *                                      ..... ④

$                                                        ..... ⑤
```

[Explanation]

①Disk 2 format.

②To initialize disk 2. (To initialize each table information)
To be displayed every time each table is initialized.

③To copy program/ system guidance.
Sector No. copying at present is displayed in real time.

④User prompt's copy.

⑤To display command prompt "$".
Copy finishes normally.

23. LMON COMMAND (Circuit condition display)

(1) Function

To display the circuit condition every 1.5 seconds on the screen. Input \ to terminate display. In the case of an ASCII screen, it is displayed only once.

(2) Operand

Nothing.

(3) How to use, example for usage

```
$ LMON
  Co No.    : Status
              1 : Ready
              2 : Ready
              3 : Error/Not Exist
              4 : Error/Not Exist
              5 : Error/Not Exist
              6 : Error/Not Exist
```

Note:

"Ready"	••• Possible to serve
"Incoming Call Service"	••• Processing arrival service
"Outgoing call Service"	••• Processing sending service
"DSP Reset Processing"	••• Processing DSP reset disposition
"PITS Connect Processing"	••• Processing PITS connect disposition
"Error/Not Exist"	••• DPS Card is not loaded.

MAINTENANCE AND TROUBLESHOOTING

1. SELF DIAGNOSTICS

The VPS executes self diagnostics when power up is executed. The power indicator informs the system conditions and the results of the diagnostics as shown in Table 5-1.

1-1. Normal Bootup

As the result of Self Diagnostics, if there is no problem in the VPS system, the operation mode follows the sequence 1 → 2 → 3 → 4 as shown in Table 5 - 1.

1-2. Hardware Error Detection

When VPS detects an abnormal condition in the hardware by Self Diagnostics, VPS executes a Blinking sequence as shown in Table 5 - 2. In this operation VPS repeats only the Blinking sequence (VPS Service is cut off). Turn off the power source, find the cause of the error, and turn on the power source again.

1-3. Warning Error Detection

When connecting with a PBX by a D-PITS line, and there is no problem with the Self Diagnostics sequence, but modular connector to connect with PBX is pulled out, the VPS should maintain the Warning condition in the sequence 1 → 2 → 3 → 4 as shown in Table 5 - 1. When Connecting the VPS to a programmed D-PITS port, the VPS is restored to operation mode from warning mode except when VPS does not have special obstacles.

1-4. Fatal Error Detection

As the result of System Initialization, when VPS detects an error as described below, Fatal Error is indicated in the sequence 1 → 2 → 3 → 4 as shown in Table 5 - 1. When VPS falls in the error condition, If stops service. Turn off the power source , find the cause of the error, then turn on the power source again.

Facts of Fatal Error
- DSP/COL card module is not installed. Microprocessor cannot gain access to DSP/COL card module.
- Data access from the hard disk drive has failed.
- Time data access from the real time clock IC has failed.

Table 5-1. The Power Indicator Blinking sequence when Power Up System Initializes.

VPS System Conditions	Data Terminal Screen	Blinking Sequence of the Power Indicator
1. Power Up		Light ON
2. Diagnostics	CARD TEST	Light ON
3. Initialize	SYSTEM SETUP 1... 2... 3...	Blinking Repeat 0.25 sec ON and 0.25 sec OFF
4. Operation Mode	** ON LINE MODE **	Light ON
5. Warning Error	** OFF LINE MODE **	Blinking Repeat 0.5 sec ON and 0.5 sec OFF
6. Fatal Error	** OFF LINE MODE **	Blinking Repeat 0.5 sec ON and 3.5 sec OFF

Table 5-2. Power Indicator Blinking sequence when Power Up Self Diagnostics.

Error Type	Data Terminal Screen	Blinking Sequence of the Power Indicator Check: The blinking interval is 6 sec.
1. RAM Error	RAM R/W ERROR !! IC30x Adr [xxxxxx]···	 The indicator blinks 2 times.
2. ROM Error	ROM ERROR :Sum Error!!	 The indicator blinks 3 times.
3. HDD Error (case–1)	DISK ERROR :Initialize Error!!	 The indicator blinks 4 times.
4. HDD Error (case–2)	DISK ERROR :No System!!	 The indicator blinks 5 times.
5. HDD Error (case–3)	DISK ERROR :Program Load Error!!	 The indicator blinks 6 times.
6. HDD Error (case–4)	DISK ERROR :Program Sum Error!!	 The indicator blinks 7 times.

2. THE ERROR RESULTS OF THE SELF DIAGNOSTICS

2-1. RAM Error

The Microprocessor gains access to system memory (IC304/IC305) on the CPU card in sequence of write after read. When VPS detects a different written value from read value, it judges RAM Error. This examination is executed to all addresses of system memory, VPS shows the wrong address and data on system memory detected as follows:

RAM R/W ERROR !!IC30 Adr[error address]
WtData[write(correct)pattern] RdData[read(error)pattern]

Descriptions : $IC30_x$

This indicates the parts number of the error memory.
It is either IC304 or IC305.

Adr[error address]
This informs the error address in the system memory.
[Error address] is shown by 8-bit code.

WtData[write(correct)pattern]
This is a correct pattern which is written into the system memory by the Microprocessor. The type of write patterns are 0, 5, A or F.

RdData[read(error)pattern]
This is an error pattern which is read from system memory.

2-2. ROM Error

The Microprocessor reads all data from system ROM (IC306/IC307) on a CPU card by a 16-bit unit, then calculates the total of the data value. VPS judges error when the sum total differs from the correct value calculated beforehand.

2-3. HDD Error

These Errors are displayed when data transfer between the Microprocessor and hard disk drive fails. HDD Error has four messages depending on the error situation.

case - 1 : DISK ERROR : Initialize Error!!

This error indicates the Microprocessor detects an abnormal status of the hard disk drive. Generally, this happens when the hard disk connecting cable is pulled out.

case - 2 : DISK ERROR : No system!!

This error indicates system program is not installed to the hard disk drive. System program should be installed to the hard disk again.

case - 3 : DISK ERROR : Program Load Error!!

This error indicates system program installed in the hard disk failed in the process of being loaded to system memory. Most likely in the process of data transfer from the hard disk drive. Generally digital logic inside the hard disk drive is out of order. In this case, replacement of the hard disk drive is necessary.

case - 4 : DISK ERROR : Program Sum Error!!

The Microprocessor reads all system programs from the hard disk to system memory by a 32-bit unit. Then it calculates the total of the data value. VPS judges Program Sum Error when the total sum differs from the correct value calculated beforehand. Generally, media inside the hard disk drive is out of order. In this case, replacement of the hard disk drive is necessary.

3. ERROR LOG FILE

The VPS system stores system errors detected during on line service in the Error Log File inside the hard disk drive. The Error Log File can be displayed on the data terminal by entering the Utility Command "ELOG". System errors detected by VPS during operation are shown in Table 5 - 3. There are two different kinds of errors, warning and fatal error. Warning error can continue to operate automatically by VPS rejecting the generated error fact by itself. In case of fatal error, VPS cannot reject the generated error fact, therefore, the VPS system falls in the condition of Off Line.

Table 5-3. Types of Errors when On Line Service.

Type	Device	Error	Descriptions
Warning	CPU	MEM-GET	This message is dependent on the system software algorithm. Hardware logic has no problem.
	DISK	DATA R/W (XX:YYYY)	There is a data transfer error between the Hard Disk Drive and the Microprocessor. XX means the error code YYYY means the error sector number
	DSPn (*1)	FIFO	Status error on a DSP card. The DSP i/f logic on the DSP card has trouble. It's i/f is between IC101 and IC109.
Fatal	CLOCK		Real Time Clock (IC308) access error.
	DSPn (*1)	SCAN	Status error on a DSP card. The Microprocessor i/f on the DSP card has trouble. It's i/f is between CN101 and IC101.
Warning or Fatal	CPU	APPLICATION (%) (%) means port No.	There is a system error. If this error is detected by the VPS, please inform.

(*1) "n" means DSP chip number in the system

n = 1 : IC109A of the DSP card in SLOT #1, n = 2 : IC109B of the DSP card in SLOT #1

n = 3 : IC109A of the DSP card in SLOT #2, n = 4 : IC109B of the DSP card in SLOT #2

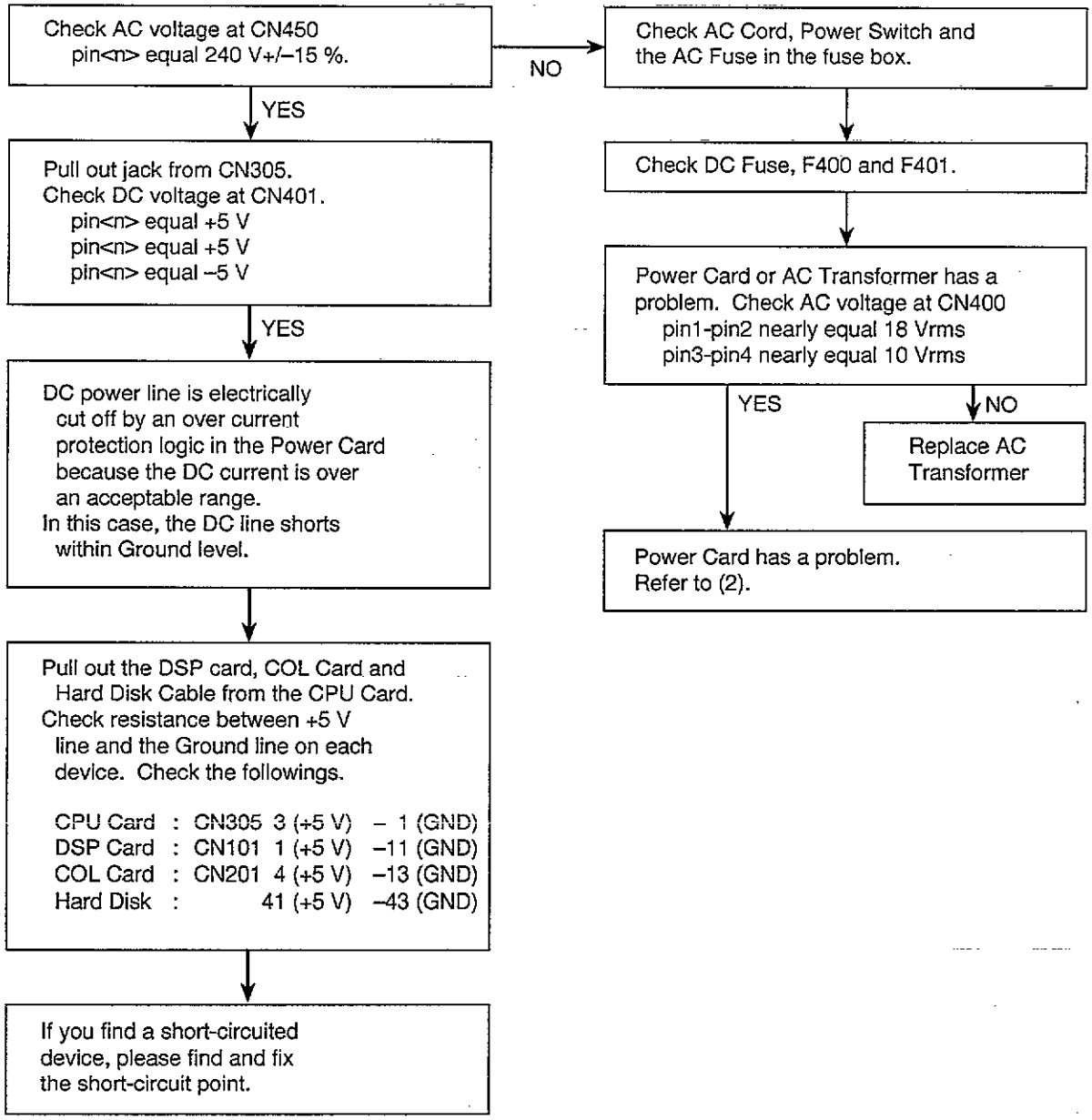
4. TROUBLESHOOTING GUIDE

This section provides the information on troubleshooting.

4-1. No Operation

(1) Power Indicator does not light up in spite of Power ON.

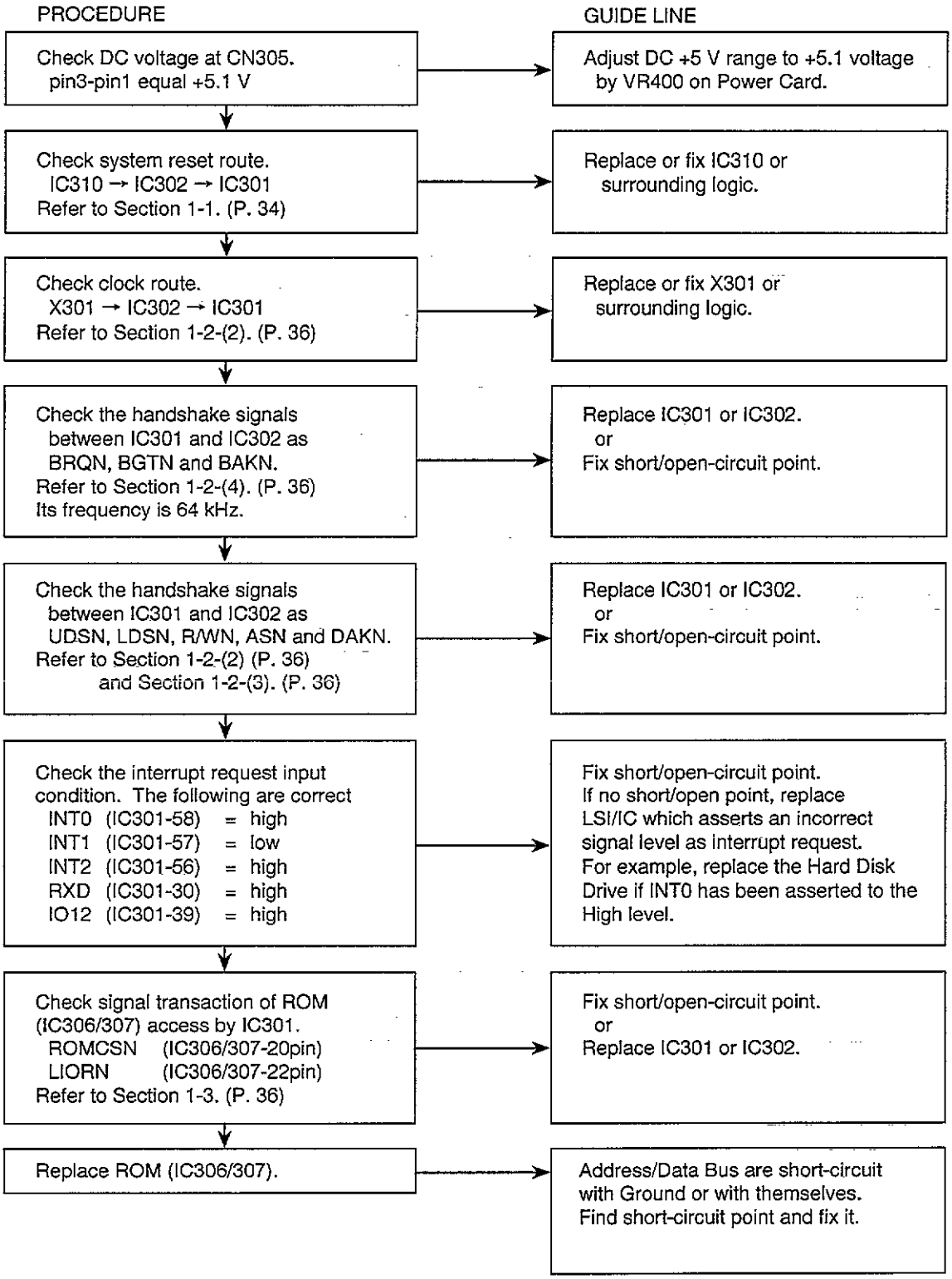
In this case, DC voltage which is supplied to CPU Card is not an acceptable range.
Check supplied DC voltage route to the CPU Card from the AC Inlet as follows.



Check : If the Hard Disk Cable is misattached to the connector on the CPU Card, +5 V line will be shorted to Ground level. Check its connection between the Cable and the CPU Card/Hard Disk Drive.

(2) The Power Indicator does not blink at the power up sequence eren though the Power Card has no Problem.

In this case, a micro processor on the CPU card does not runn on a ROM based-program.



(3) *The Power Indicator informs the Hardware Error by the blinking sequence at the power up self diagnostic.*
Please refer to Section 1-(2) (P. 82) and Section 2. (P. 83)

In this case, the CPU Card or Hard Disk Drive has a problem. Please connect the Data Terminal to the VPS, and restart the system. The Data Terminal provides an error status on the screen display.

SCREEN DISPLAY on a Data Terminal and Procedure	GUIDE LINE
RAM R/W ERROR IC304/305 or an around logic has a problem. Refer to Section 1-4. (P. 41) Check voltage to system memory. IC304/305pin-1, 14 = +5 V Check the control signal transaction as RASON, CASN, MOEN, LWEN and UWEN. There are driven by IC302. Check memory address bus transaction as MA <9-0>. They are driven by IC302. Replace IC304 or IC305.	Check +5 V pattern Replace IC302 if IC302 does not assert the control signals. or Fix short-circuit point.
ROM ERROR IC306/307 has a problem. Please refer to Section 1-3. (P. 39) ROM interface logic is no problem because a Microprocessor is running on this ROM (IC306/307) based program. Replace IC306 or IC307, and then restart.	If failure occurs in spite of replacing IC306/307. The higher address bus line is short with +5 V, ground or themselves. Fix short-circuit point.
DISK ERROR: Initialize Error!! Hard Disk Drive or interface logic on the CPU Card has a problem. Refer to Section 1-9. (P. 53) Check the connection between the HDD and CPU. Replace Hard Disk Drive and restart. Check the signal transaction of CN301. RESET, CS <1-0>, IOR, IOW, A <2-0> and D <15-0>.	Re-attach a disk cable. Fix short/open- circuit point or Replace driver ICs as IC312, 313, 314 and 315.

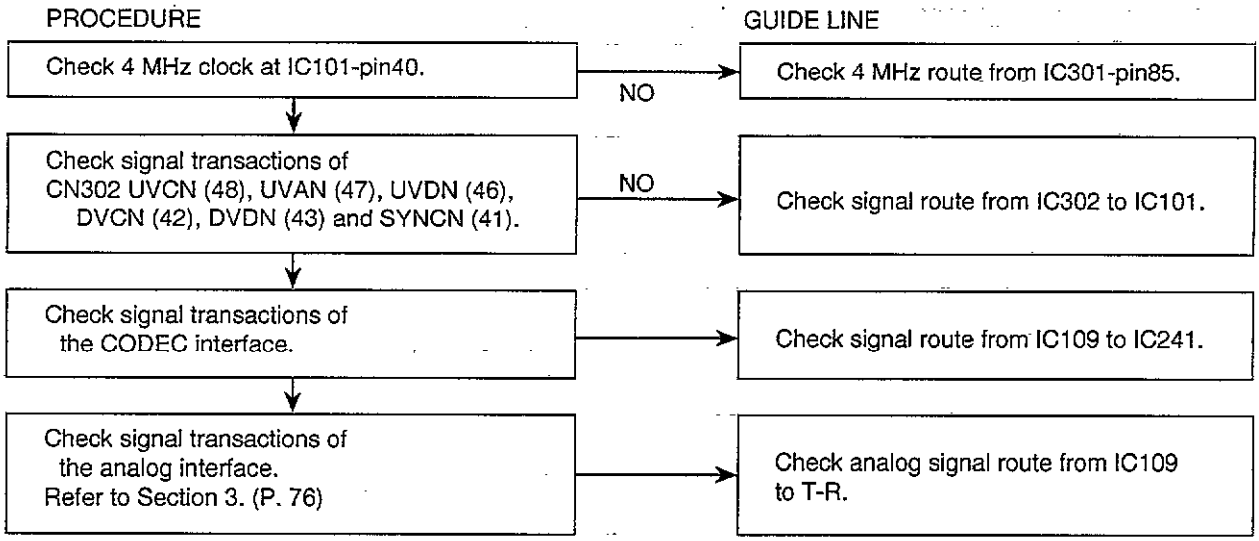
DISK ERROR: No System!! Hard Disk Drive is not installed to a system program.	→ Install a system program by using an Utility Com'd.
DISK ERROR: Program Load Error!! Microprocessor failed to load a system program from the Hard Disk Drive.	→ Replace Hard Disk Drive.
DISK ERROR: Program Sum Error!! A loading program has an error pattern. It is a strange media error in the drive.	→ Replace Hard Disk Drive.
No CO Cards are active!! The expansion bus interface on the CPU Card or DSP Card has a problem. At first, find a error card by replacing the CPU and DSP Card. If the CPU Card has a problem., Check the expansion bus interface Refer to Section 1-10. (P. 57) If the DSP Card has a problem, confirm ELOG file by Data Terminal. If SCAN Error, check the CPU Card interface. Refer to Section 2-2. (P. 71) If FIFO Error, check the DSP interface. Refer to Section 2-3 (P. 71) and 2-4. (P. 71)	→ Fix short/open-circuit point. Replace driver ICs as IC316, 317 or 318. Replace driver ICs as IC102, 103, 104 or 105. Replace ROM or DSP as IC107, 108 or IC109.

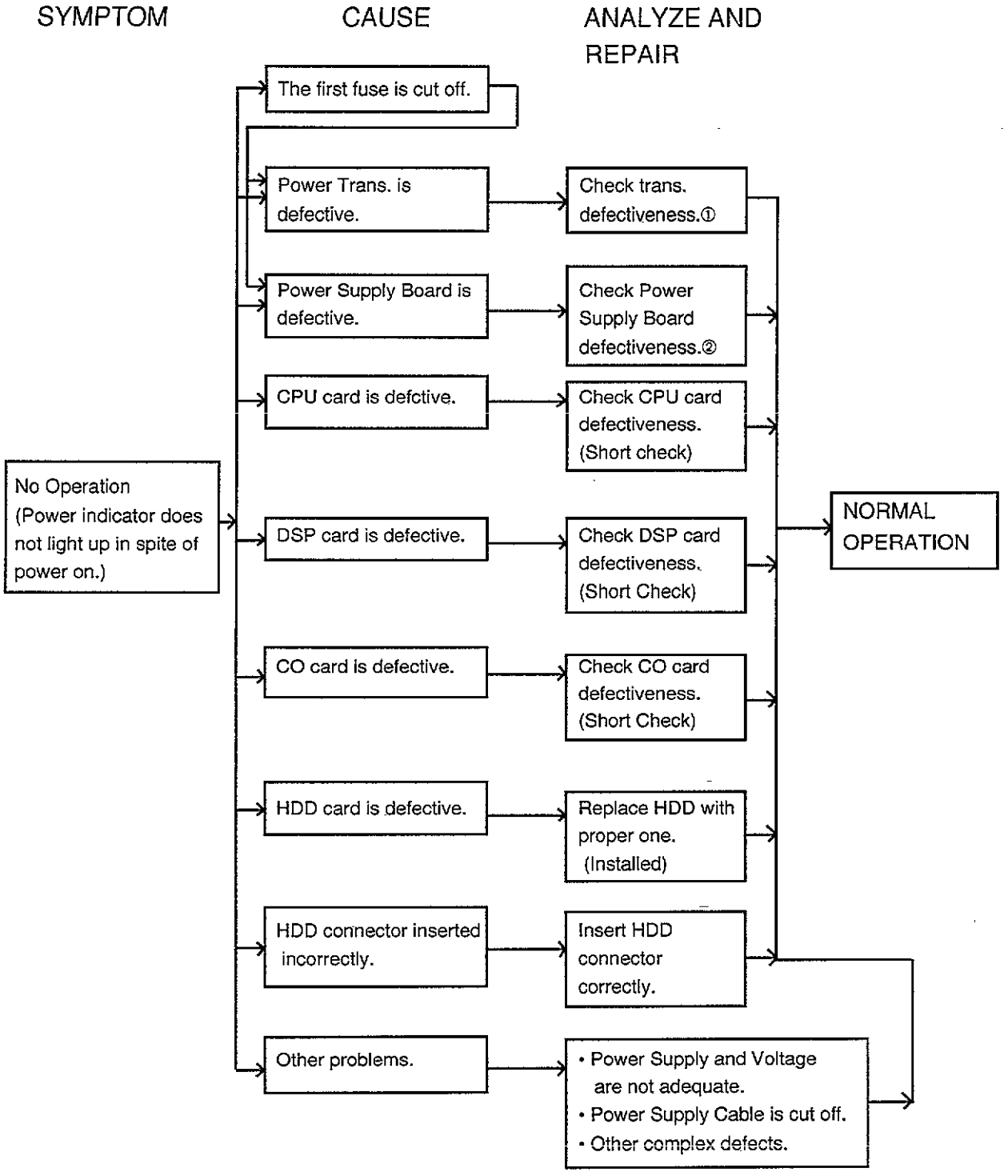
(4) The ELOG file has a message in the Hardware Error at the On Line Service.
Please refer to Section 3. (P. 83)

SCREEN DISPLAY on the Data Terminal and Procedure	GUIDE LINE
DISK DATA R/W (XX:YYYY) There is a data transfer error between the Drive and Microprocessor on the CPU Card. Refer to Section 1-9. (P. 53) Check the connection between the HDD and CPU. Replace Hard Disk Drive and then restart. Check the signal transaction of CN301. RESET, CS <1-0>, IOR, IOW, A < 2-0 > and D <15-0>.	Re-attach the disk cable. Fix short/open-circuit point or Replace driver ICs as IC312, 313, 314 and 315
DSPn FIFO Status error in the DSP Card. The DSP interface logic has a problem. It is between CN101 and IC101. Refer to Section 2-3 (P. 71) and 2-4. (P. 71)	Replace ROM or DSP as IC107, 108 or IC109.
DSPn SCAN Status error in the DSP Card. The CPU Card interface has a problem. It is between CN101 and IC101. Refer to Section 2-2. (P. 71)	Replace driver ICs as IC102, 103, 104 or 105.
CLOCK The Real Time Clock IC (IC308) has an access error. Refer to Section 1-7. (P. 48)	Replace IC308.

(5) The VPS can not receive/transmit messages from/to PBX.

In this case, the data transfer route of the voice message has a problem. Its route is the serial voice port between the CPU Card and DSP Card. Refer to Section 1-10-(5). (P. 57)



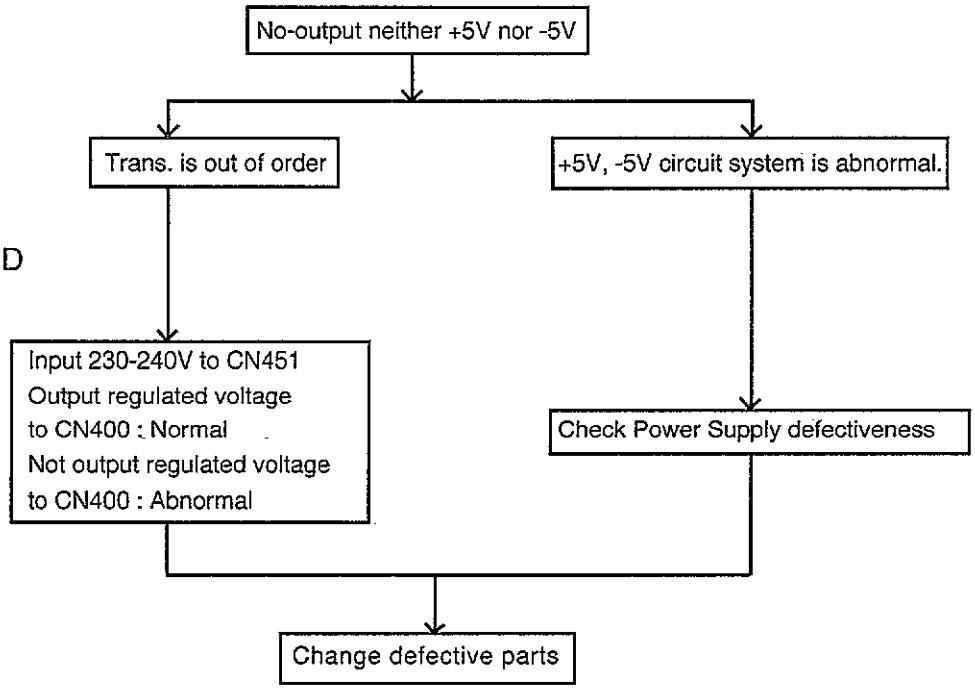

SYMPTOM
CAUSE
ANALYZE AND REPAIR
No Operation (Power indicator does not light up in spite of power on.)
The first fuse is cut off.
Power Trans. is defective.
Check trans. defectiveness.①
Power Supply Board is defective.
Check Power Supply Board defectiveness.②
CPU card is defctive.
Check CPU card defectiveness. (Short check)
DSP card is defective.
Check DSP card defectiveness. (Short Check)
CO card is defective.
Check CO card defectiveness. (Short Check)
HDD card is defective.
Replace HDD with proper one. (Installed)
HDD connector inserted incorrectly.
Insert HDD connector correctly.
Other problems.
• Power Supply and Voltage are not adequate.
• Power Supply Cable is cut off.
• Other complex defects.
NORMAL OPERATION

①TRANS. DEFECTS

SYMPTOM

CAUSE

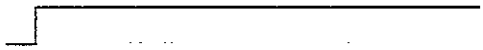
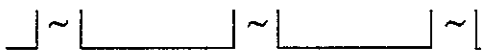
ANALYZE AND REPAIR



Power LED's ON and OFF is abnormal

<POWER LED ON and OFF pattern>

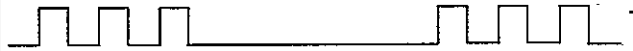
[Normal LED ON and OFF pattern]

Phase	Screen Display	LED Condition
Power ON		ON 
System Data is under construction	System Set up	ON and OFF  0.25 second 0.25 second
After start up		
May apply	** ON LINE MODE **	ON  → Normal
May not apply (1)	** OFF LINE MODE **	ON and OFF  → ③ 0.5 second 0.5 second
May not apply (2)	** OFF LINE MODE **	ON and OFF  → ④ 0.5 second 3.5 second

Remarks May not apply (1) is the condition of PITS communication circuit being out, can recover condition.
May not apply (2) is No CO/DSP card or error generation in starting up, etc. with serious error and cannot recover.

[LED ON and OFF pattern at generated error]

In case an error generates from the time Power Source is ON in to system data in under construction, the LED displays as follows.

Error	Screen Display	LED Condition
DC Alarm		ON and OFF  → ⑤
RAM error		ON and OFF  → ⑥
ROM error	ROM ERROR : Sum Error!!	ON and OFF  → ⑦
HDD error (Initialize)	DISK ERROR : Initialize Error!!	ON and OFF  → ⑧
HDD error (No-system)	DISK ERROR : No System!!	ON and OFF  → ⑨
HDD error (Read in error)	DISK ERROR : Program Load Error!!	ON and OFF  → ⑩
HDD error (Check sum)	DISK ERROR : Program Sum Error!!	ON and OFF  → ⑪

②POWER SUPPLY BOARD DEFECT CHART - 1

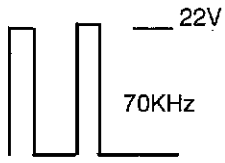
SYMPTOM

+5V is not output.

CAUSE

F400 fuse is cut off.	IC400 DC-DC converter is defective.	Over current detection works.

ANALYZE AND REPAIR

• Check Point Check +5V system circuit board, part's short.	• Check Point There is about 25V input to IC400 - 3. IC400 - 2  is output, then it's normal. Abnormal causes 1. Short defects in the IC400 lead line and its control parts. 2. IC400 is defective.	• Check Point Check Circuit, Board part's short after DC-DC converter.
Change or repair defective parts and place.	Repair defect. Change IC400.	Change or repair defective parts and place.

②POWER SUPPLY BOARD DEFECT CHART - 2

SYMPTOM

+5V is not output.

CAUSE

+5 over voltage detection works.	Heating detection of DC-DC converter works.	Q1 transistor is defective.	Other defects soldering, parts, etc.
ANALYZE AND REPAIR			
• Check Point Q2 is off. Base of Q2 "L" : Over voltage motion "H" : Normal • Abnormal cause 1. IC400 defect causes the generation of over voltage. 2. False of over voltage detective circuit.	• Check Point +5V output stops, when IC 400 is over heated or in process of heating. When the temperature of IC400 goes down, +5V is outputted. It is abnormal that +5V output is repeatedly on and off depending on IC400's heating system described above. Cause of abnormal 1. Control pin of IC400 is shorted. 2. VR408, R410 the parts for control voltage are short. 3. IC is not enough attatched to heat sink.	• Check Point Q2 is ON. But voltage is not outputted to Q1 collector. YES : Normal NO : Abnormal	Check voltage and waveform of circuit diagram's check point , then analyze and repair surrounding parts.
Change or repair defective parts and place.	Repair defective place. Adjust installation of IC400.	Repair defective parts. Change Q1.	Change or repair defective parts and place.

②POWER SUPPLY BOARD DEFECT CHART - 3

SYMPTOM

-5V is not output.

CAUSE

F401 fuse is cut off

IC401 regulator is defective.

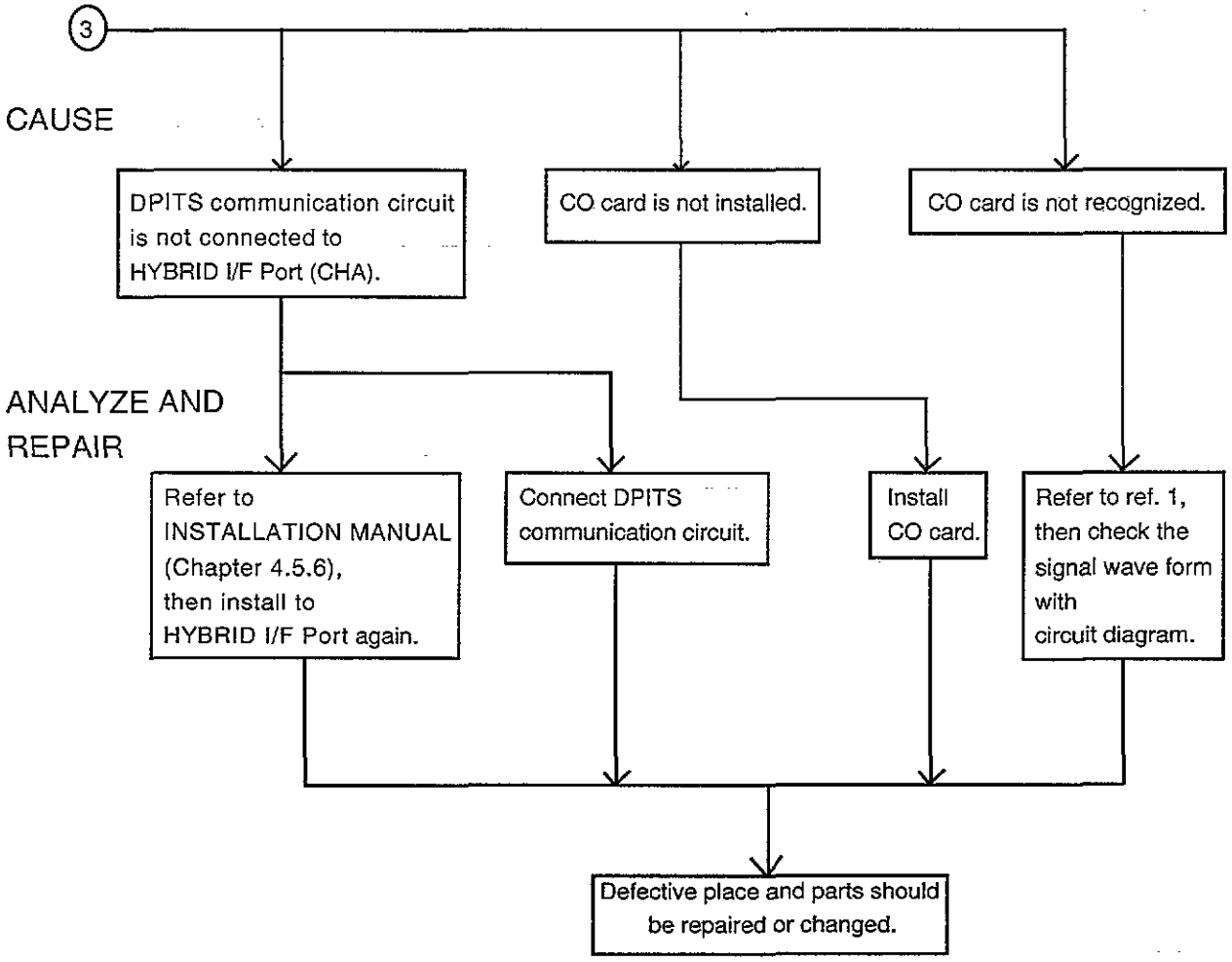
Check -5V system circuit's short and abnormality.

At IC401①, there is -10V input and to ②-5V is output
YES : Normal
No : Abnormal

ANALYZE AND REPAIR

Change the defective parts.

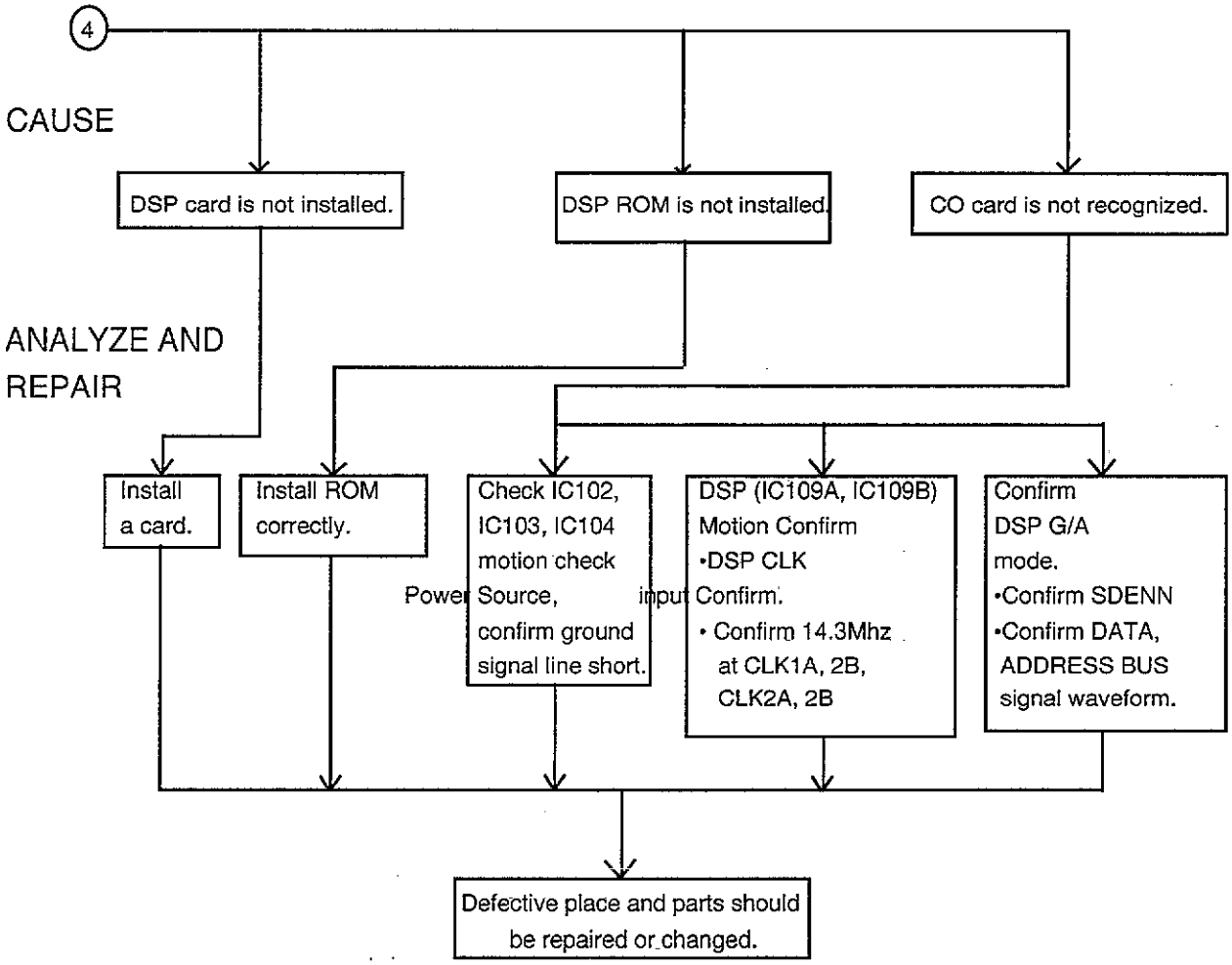
After power on, LED's ON and OFF is abnormal



Terminal Display Example

```
CARD TEST . . .

SYSTEM SETUP . . .

   1. .        2. .        3. .

   Active COs          :  1 2
   DPITS Interface Connection is not Established

** OFF LINE MODE **
```

After power on, LED's ON and OFF is abnormal



Terminal Display Example

```
>
CARD TEST . . .

SYSTEM SETUP . . .

    1. .        2. .        3. .

    No CO line cards are active !!


* * OFF LINE MODE * *
```

After power on, LED's ON and OFF is abnormal

⑤ To detect DC Alarm

CAUSE

- DC alarm dection circuit is defective.
- +5V voltage is low.

ANALYZE AND REPAIR

- DC alarm detection circuit check.
  - Check Point
    - Q5 (4AP)
    - D405 (4AP)
    - CN401⑤ (4AP)
  - Check mode along with the circuit diagram.
- Adjust the voltage at VR400.
  If there is more than 5.10v on CPU board on install condition.

→ Defective place and parts should be repaired or changed.

After power on, LED's ON and OFF is abnormal

⑥ Cannot read or write with RAM

CAUSE

- RAM (IC304, IC305) and surroundings are defective.

ANALYZE AND REPAIR

- Check Point
  - IC304, IC305 ⑦, ⑧, ㉒, ㉓
    ↗ ↗ ↗ ↗
    $\overline{WE}$, $\overline{RAS}$, $\overline{OE}$, $\overline{CAS}$
  - DATA, ADDRESS BUS

→ Defective place and parts should be repaired or changed.

After power on, LED's ON and OFF is abnormal

(7) Cannot read or write with ROM

CAUSE

ROM (IC306, IC307) and surroundings are defective.

ANALYZE AND REPAIR

Check Point
- IC306, IC307 (20), (22)
  - (20) → CEN
  - (22) → OEN
- DATA, ADDRESS BUS

Defective place and parts should be repaired or changed.

After power on LED's ON and OFF is abnormal

(8) HDD doesn't work. (H.D.D. initialize error.)

CAUSE

- HDD is not installed.
- HDD is broken.
- HDD interface part is defective.

ANALYZE AND REPAIR

- Install HDD. (HDD Connection Check)
- Replace with new HDD.
- Check interface part's motion along with the circuit diagram. IC314, IC312, IC313,IC315, LDDIR, HDENN

Defective place and parts should be repaired or changed.

After power on, LED's ON and OFF is abnormal

(9) Software inside HDD is broken. (No-system)

CAUSE

- Software inside HDD is broken.
- HDD interface part is broken.

ANALYZE AND REPAIR

- Install new software again.
- Check interface part motion along with circuit diagram. IC314, IC312, IC313, IC315 LDDIR, HDENN
- Defective place and parts should be repaired or changed.

After power on, LED's ON and OFF is abnormal

(10) Application program inside HDD cannot be read.

CAUSE

- Application program inside HDD is broken.
- HDD interface part is broken.

ANALYZE AND REPAIR

- Install new software again.
- Check interface part motion along with circuit diagram. IC314, IC312, IC313, IC315 LDDIR, HDENN
- Defective place and parts should be repaired or changed.

After power on LED's ON and OFF is abnormal

(11) Program check sum inside HDD cannot be completed.

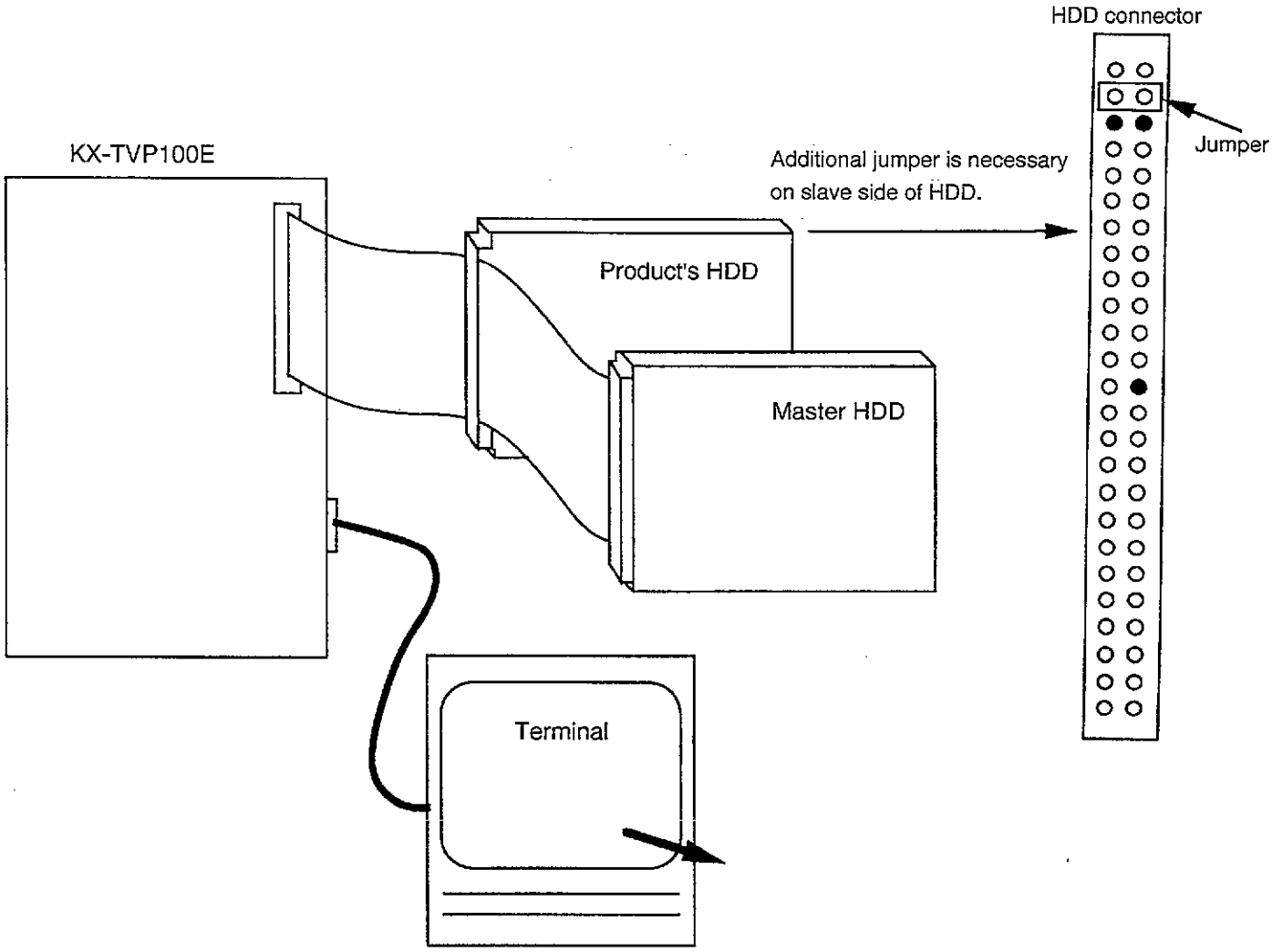
CAUSE

Software inside HDD is broken.

ANALYZE AND REPAIR

Install new software again.

HDD INSTALLATION PROCEDURE



1. To start up with POWER ON Master HDD.
2. Select "1. ASCII TERMINAL" as Terminal Type.
3. Select "3. Utility Command".
4. Input "KME" and password. (PANASONIC)
5. Input command "SYSD". (Refer to page 95)
6. Data copy is complete after 10 minutes.
7. Put HDD, HDD cable back, then start up with power on.
8. Select the destination with command "PDCT".
9. Installation is complete with Power off — Power on. Can be used.

MEMO

MEMO

SCHEMATIC DIAGRAM

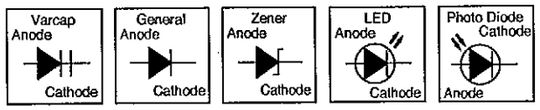
Notes:

1. DC voltage measurements are taken with an electronic voltmeter and oscilloscope from a ground line.

   (• Power Switch ON condition
   • Voltage Value : V)

2. This schematic diagram may be modified at any time with the development of new technology.

3. Important safety notice
   The shaded area on this schematic diagram incorporates special features important for protection from fire and electrical shock hazards. When servicing it is essential that only manufacturer's specified parts be used for the critical components in the shaded areas of the schematic.

4. 

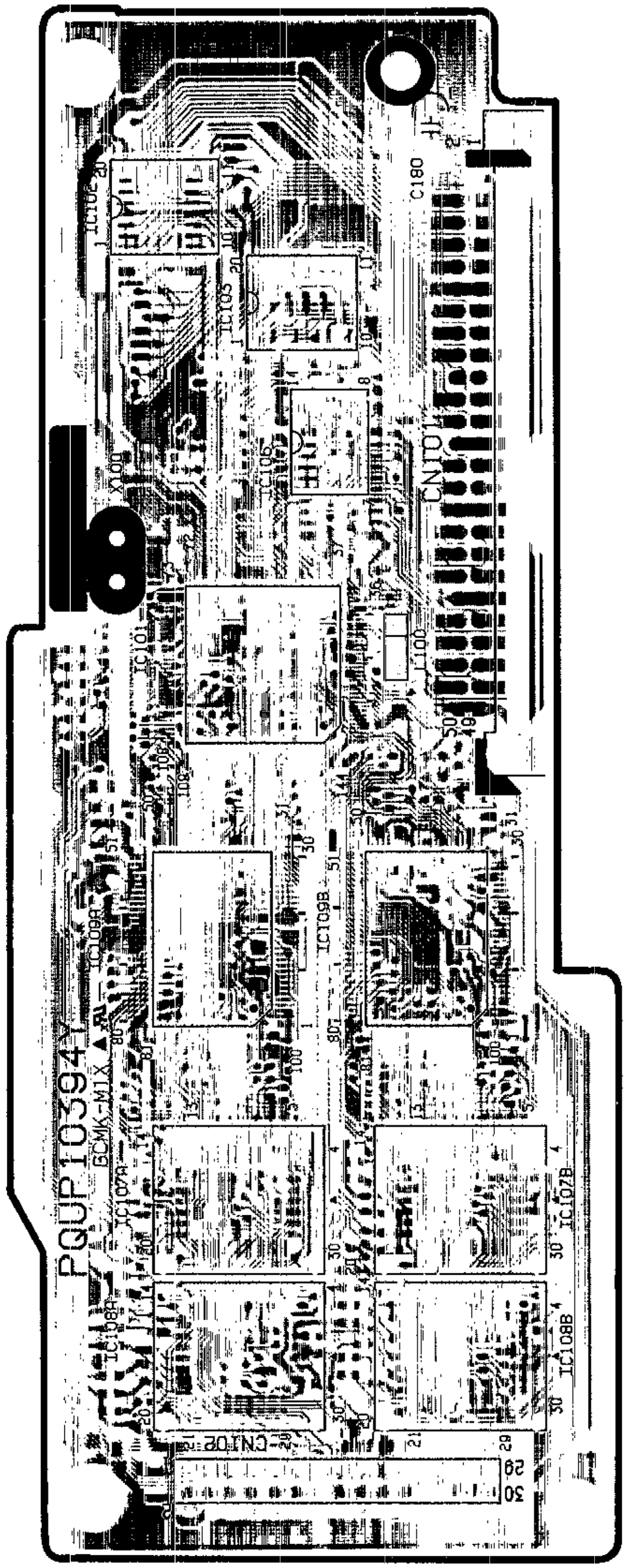
SCHEMATIC DIAGRAM (DSP)

No Mounted Device Table

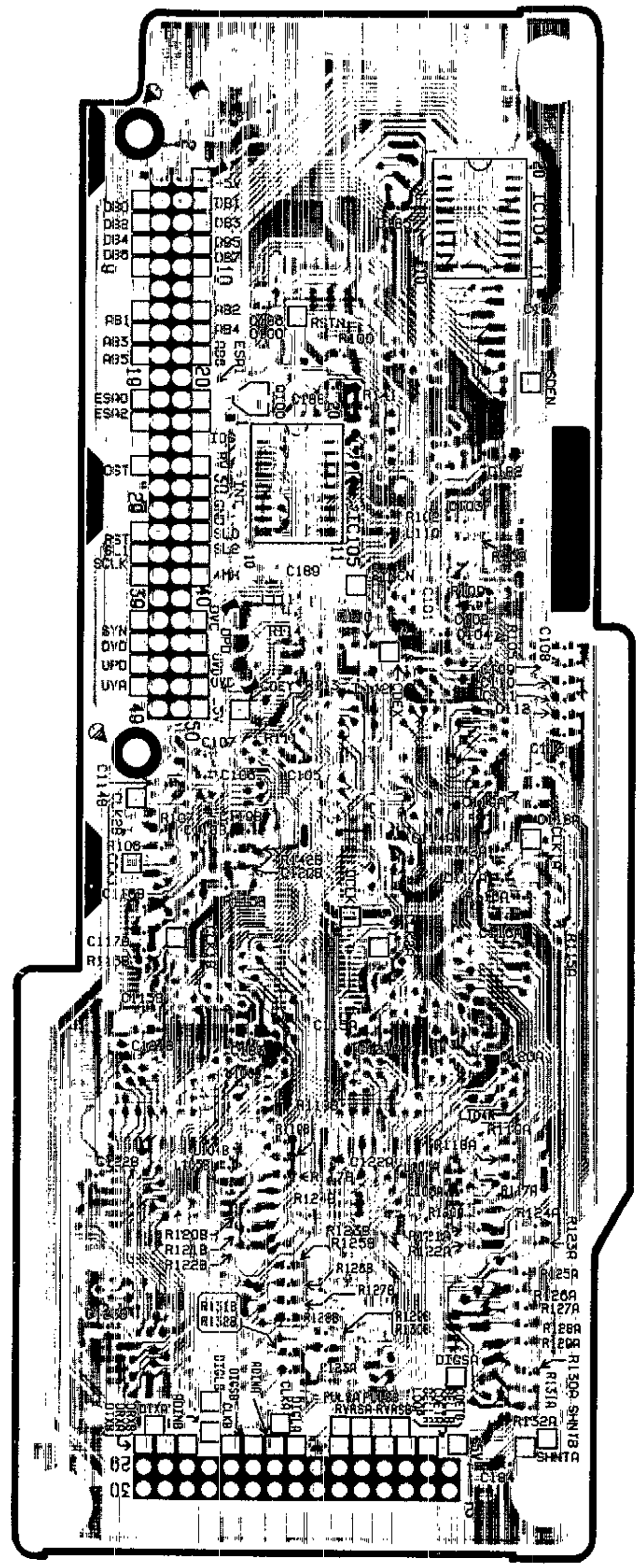
Type	Parts ID.
IC	
R	R107, R109
C	C106, C107, C108, C109, C110, C111, C112, C113
Q, D, SC	
etc	L100

PRINTED CIRCUIT BOARD (DSP)

(COMPONENT VIEW)



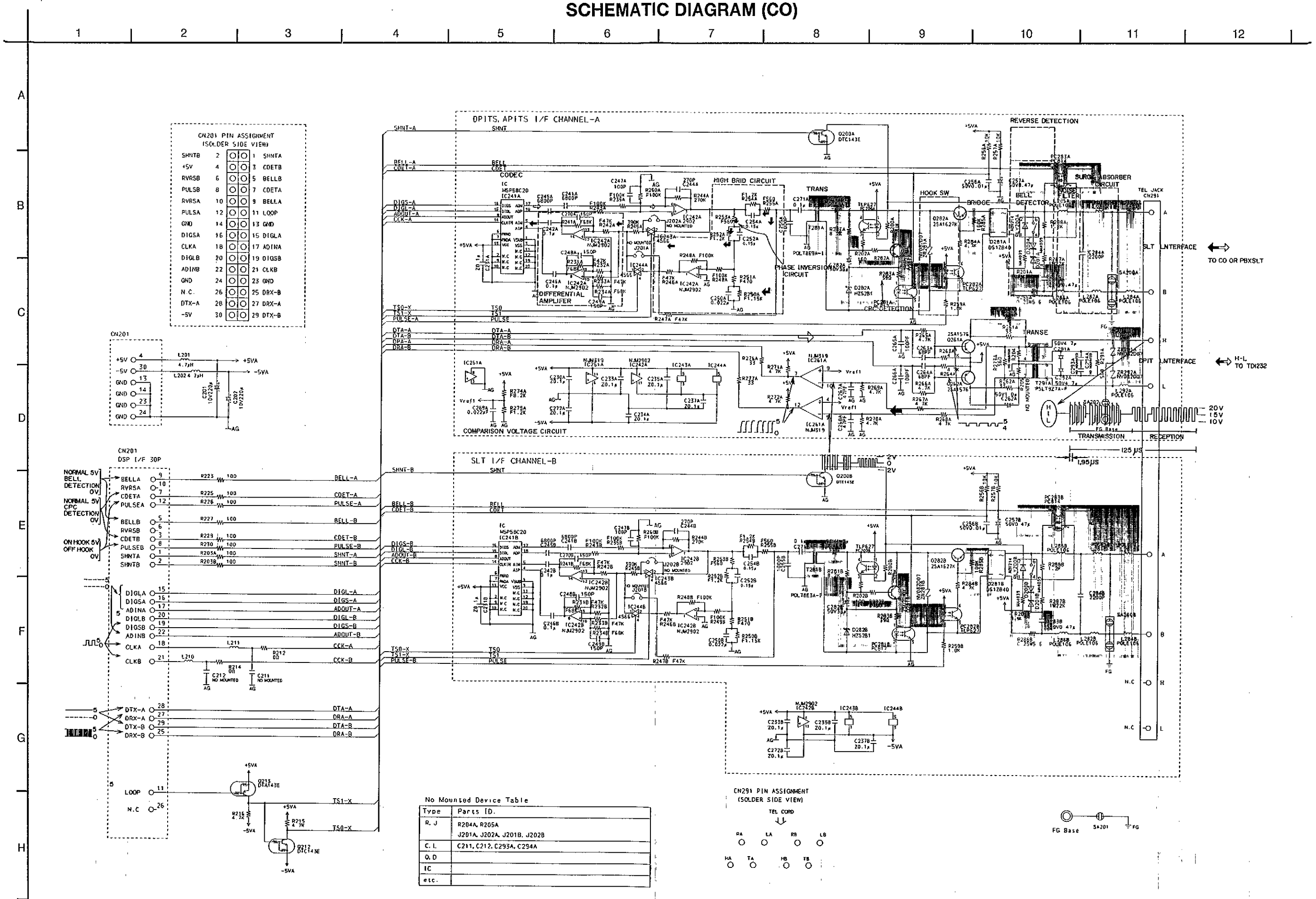
(BOTTOM VIEW)



Notes:

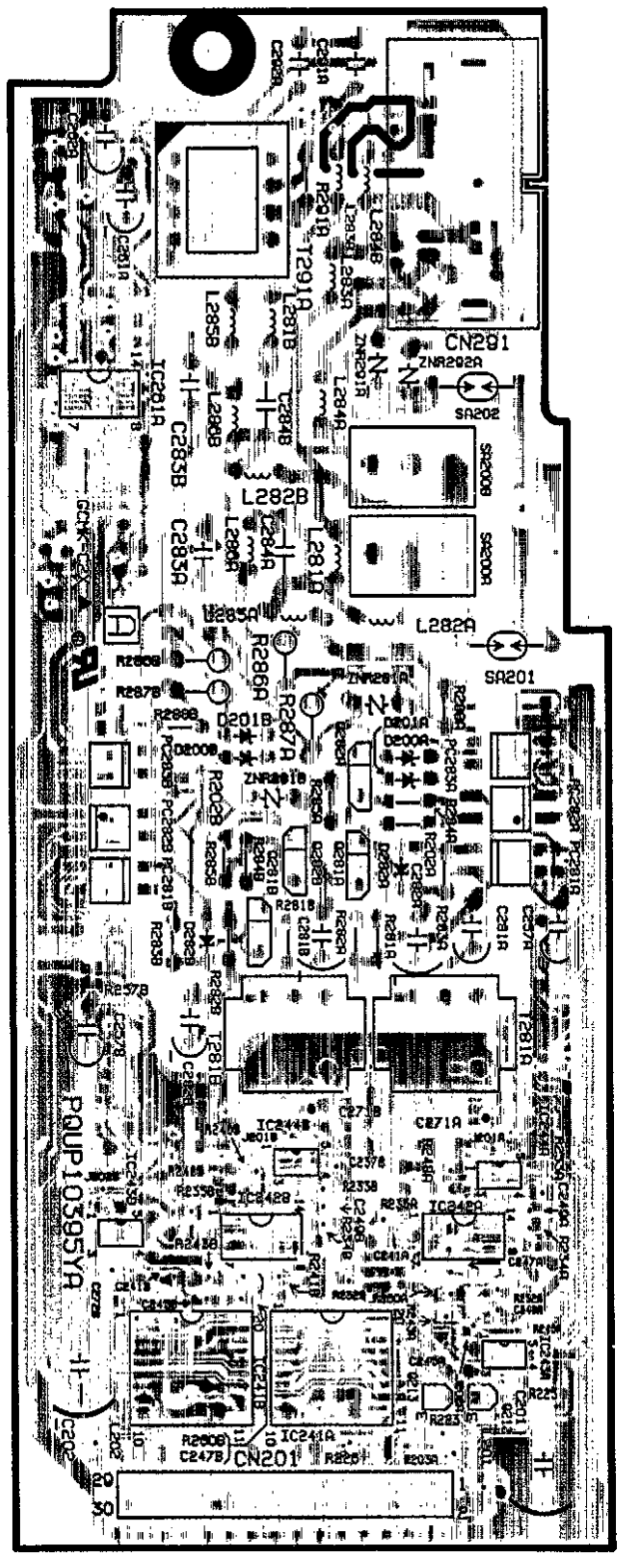
1. The circuit shown in ▭ on the conductor indicates printed circuit on the back side of the printed circuit board.
2. The circuit shown in ▭ on the conductor indicates printed circuit on the front side of the printed circuit board.
3. The circuit board may be modified at any time with the development of new technology.

SCHEMATIC DIAGRAM (CO)

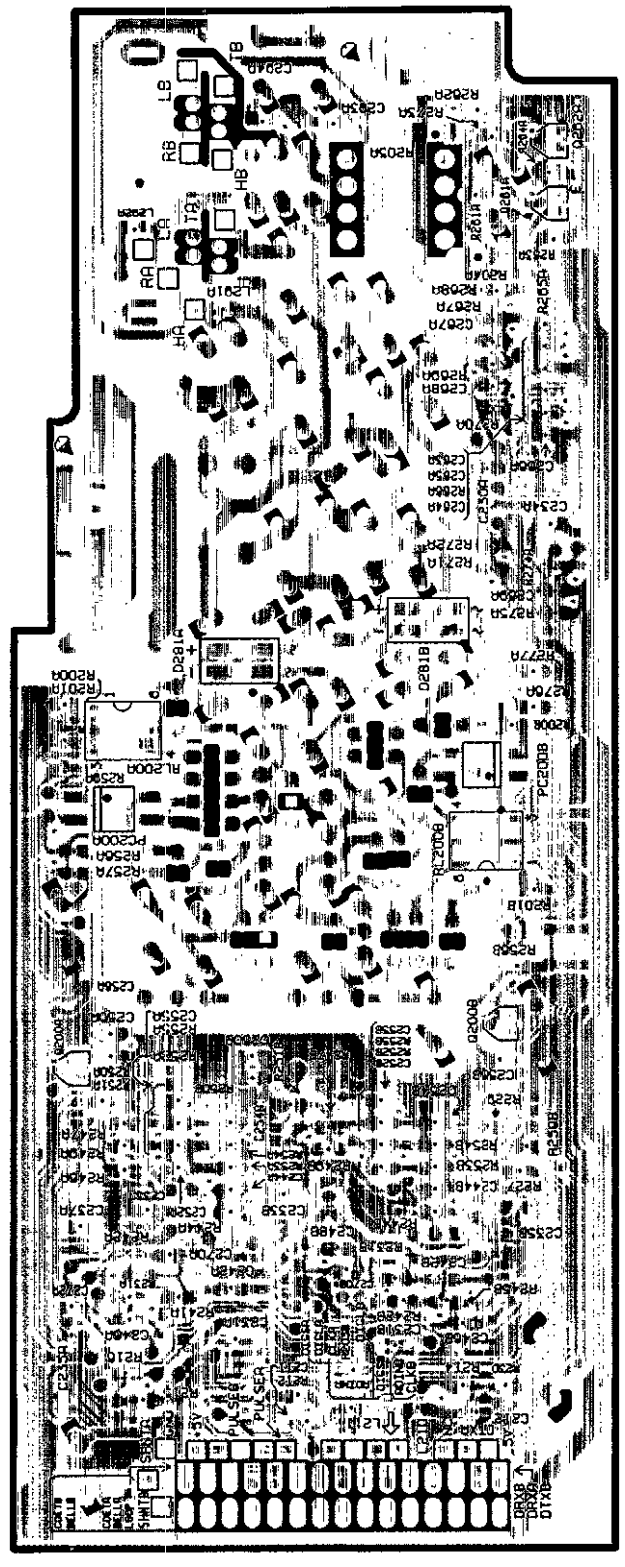


PRINTED CIRCUIT BOARD (CO)

(COMPONENT VIEW)



(BOTTOM VIEW)

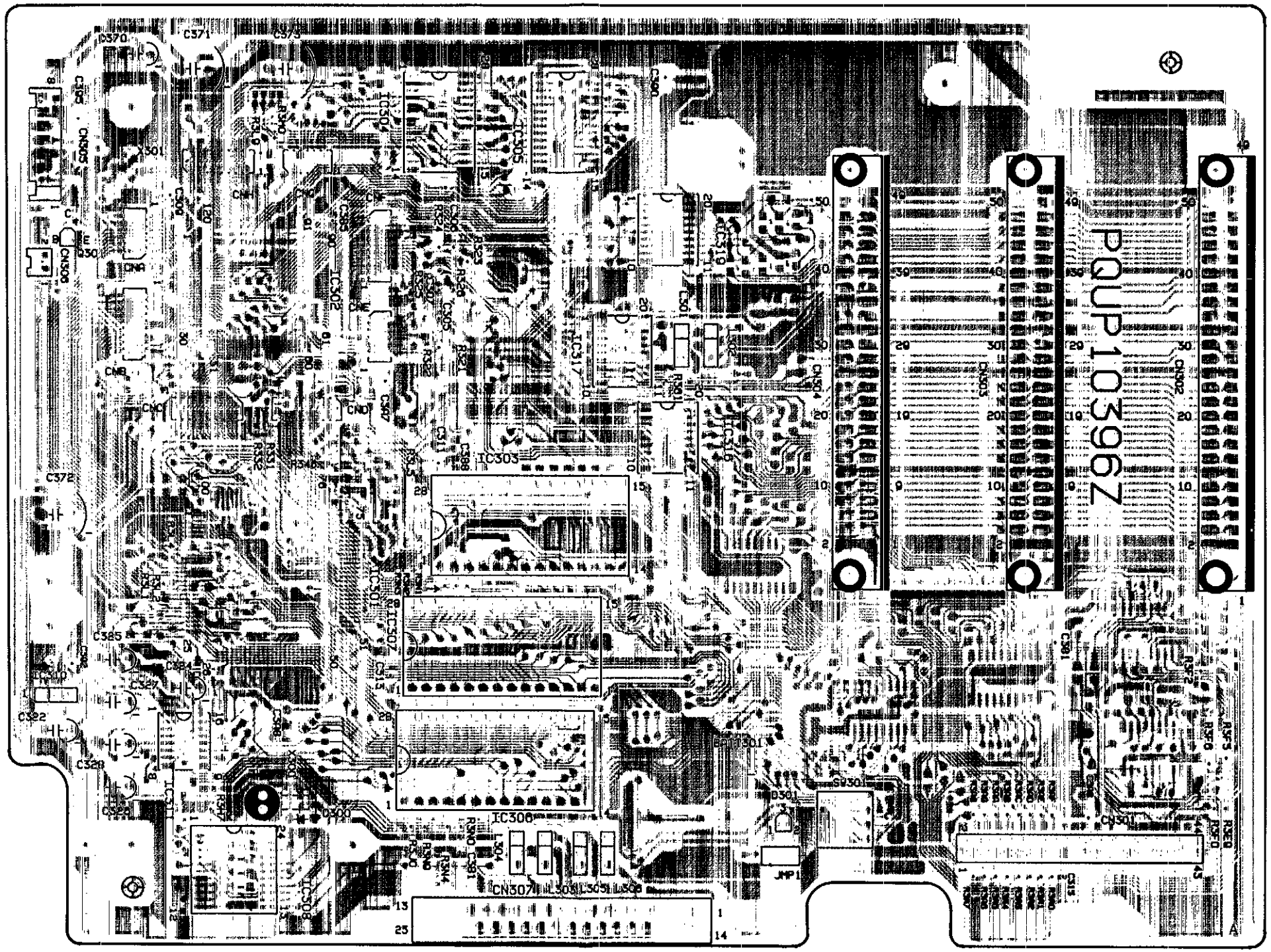


Notes:

1. The circuit shown in ▭ on the conductor indicates printed circuit on the back side of the printed circuit board.
2. The circuit shown in ▭ on the conductor indicates printed circuit on the front side of the printed circuit board.
3. The circuit board may be modified at any time with the development of new technology.

PRINTED CIRCUIT BOARD (CPU)

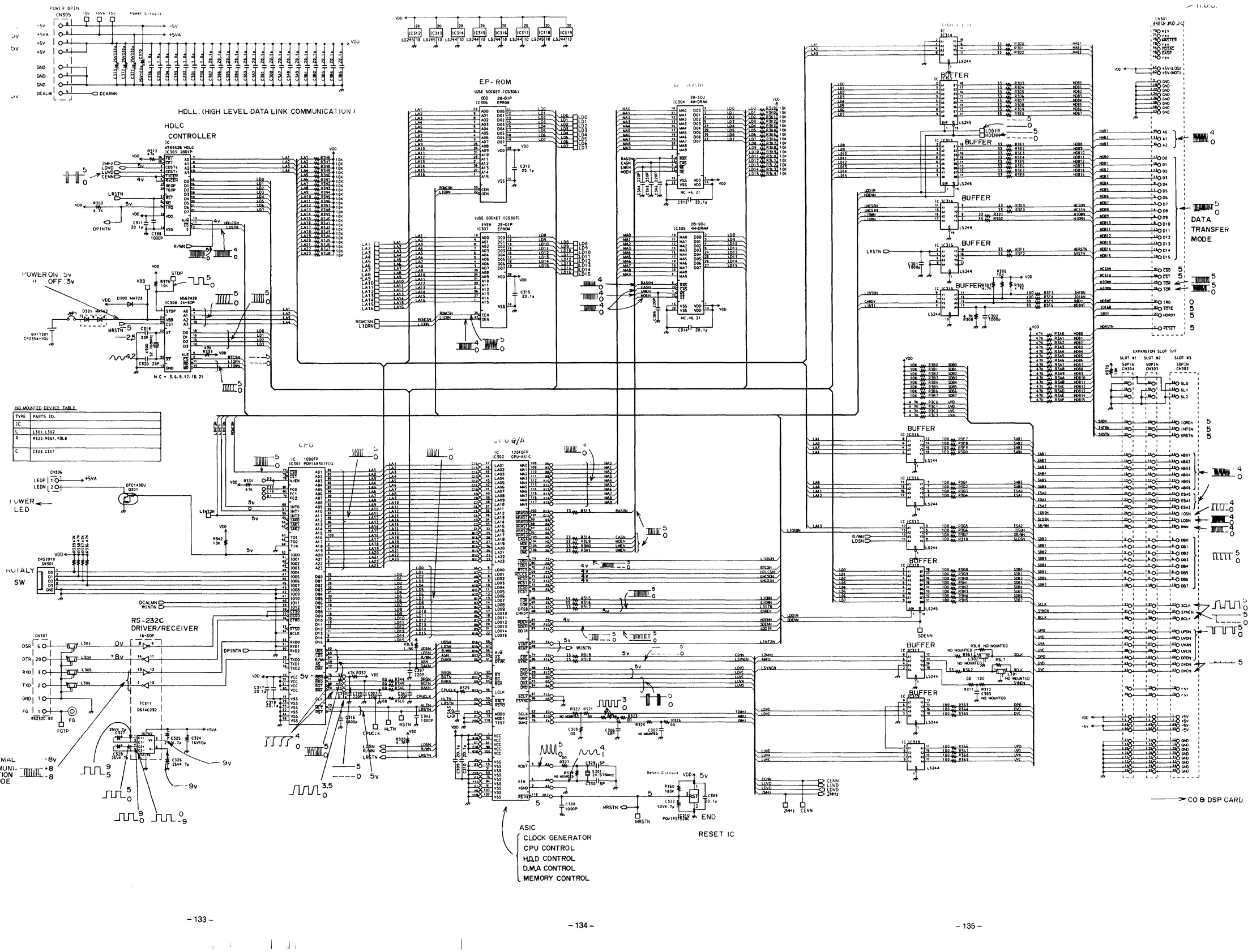
(COMPONENT VIEW)



Notes:

1. The circuit shown in ▭ on the conductor indicates printed circuit on the back side of the printed circuit board.
2. The circuit shown in ▭ on the conductor indicates printed circuit on the front side of the printed circuit board.
3. The circuit board may be modified at any time with the development of new technology.

SCHEMATIC DIAGRAM (CPU)

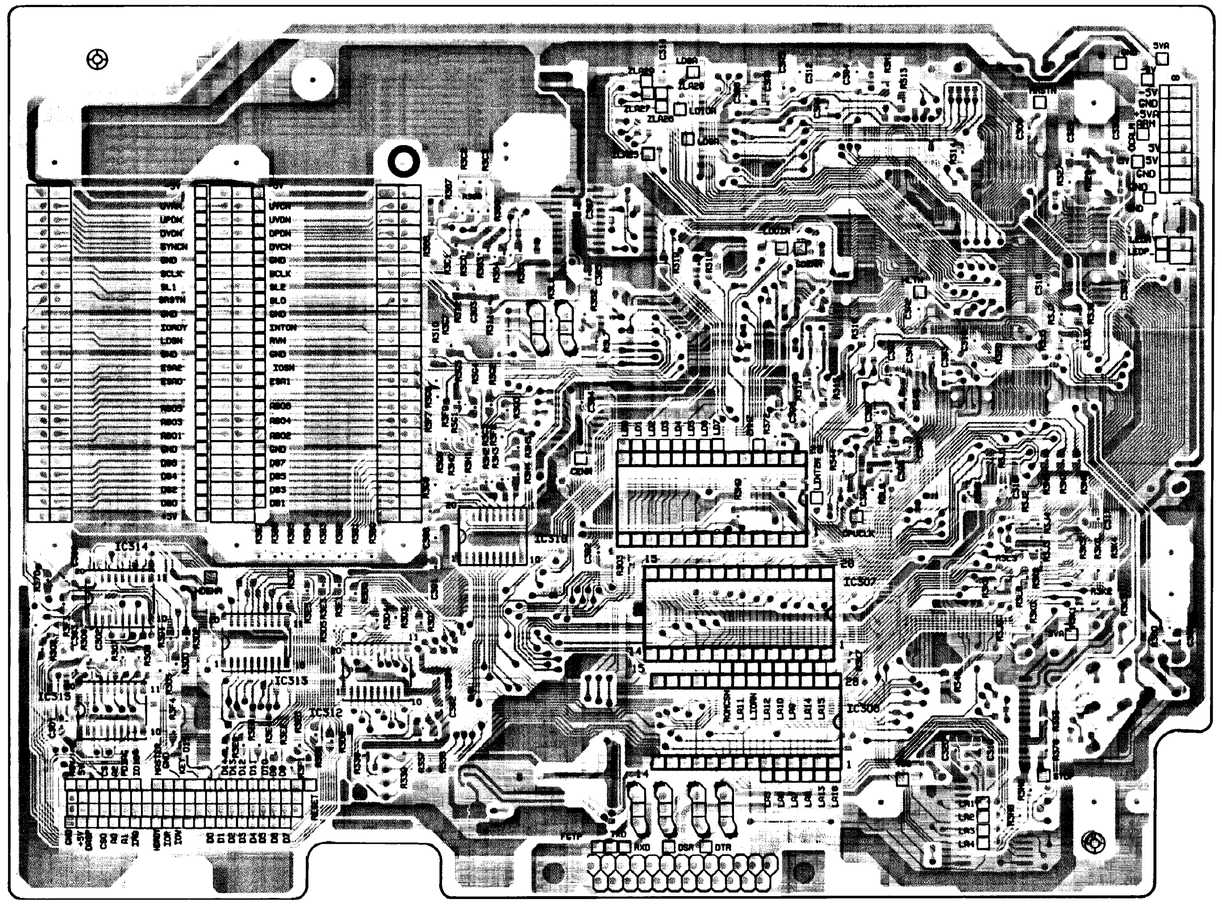


NO MOUNTED DEVICE TABLE

TYPE	PARTS ID.
IC	
L	L301, L302
R	R322, R361, R3L8
C	C301, C307

PRINTED CIRCUIT BOARD (CPU)

(BOTTOM VIEW)

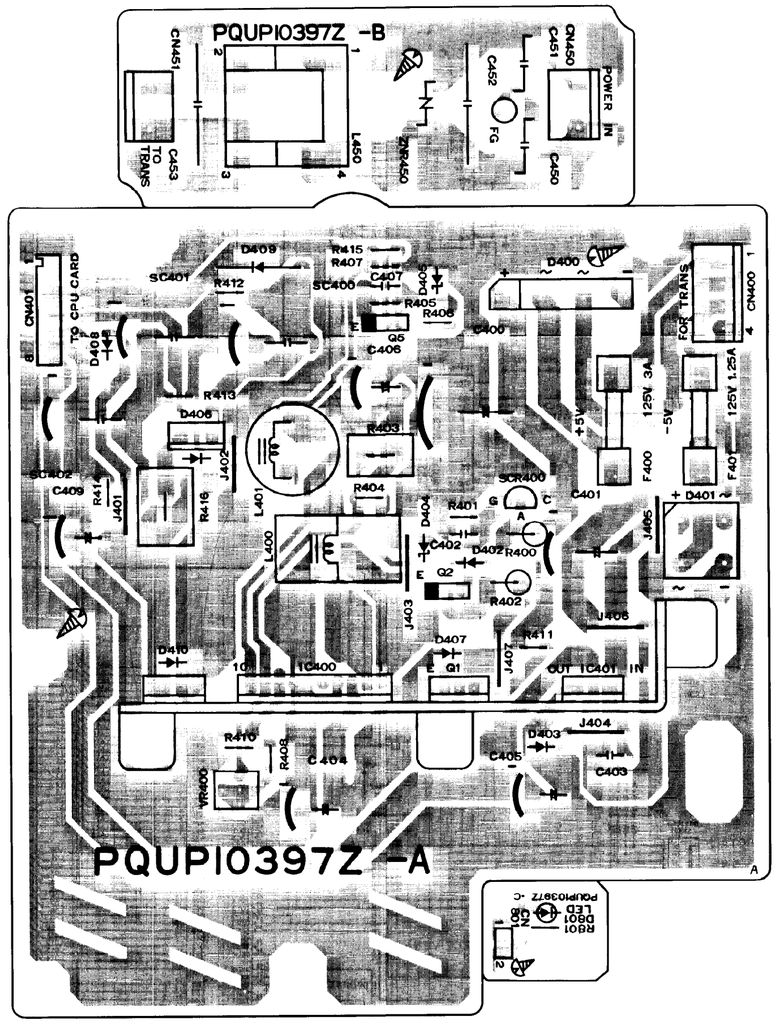


Notes:

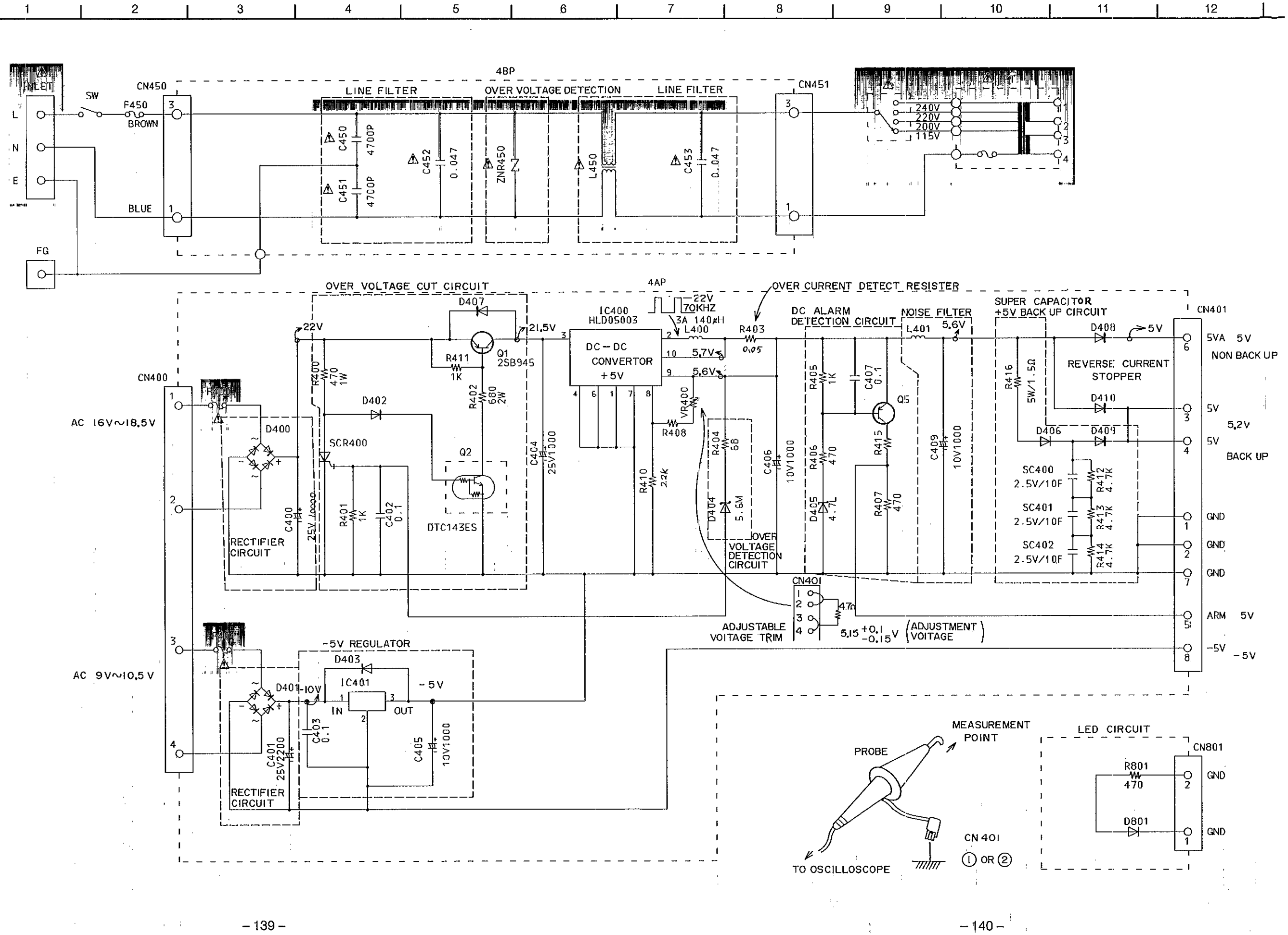
1. The circuit shown in ▭ on the conductor indicates printed circuit on the back side of the printed circuit board.
2. The circuit shown in ▭ on the conductor indicates printed circuit on the front side of the printed circuit board.
3. The circuit board may be modified at any time with the development of new technology.

PRINTED CIRCUIT BOARD (AC/DC POWER AND LED)

(COMPONENT VIEW)

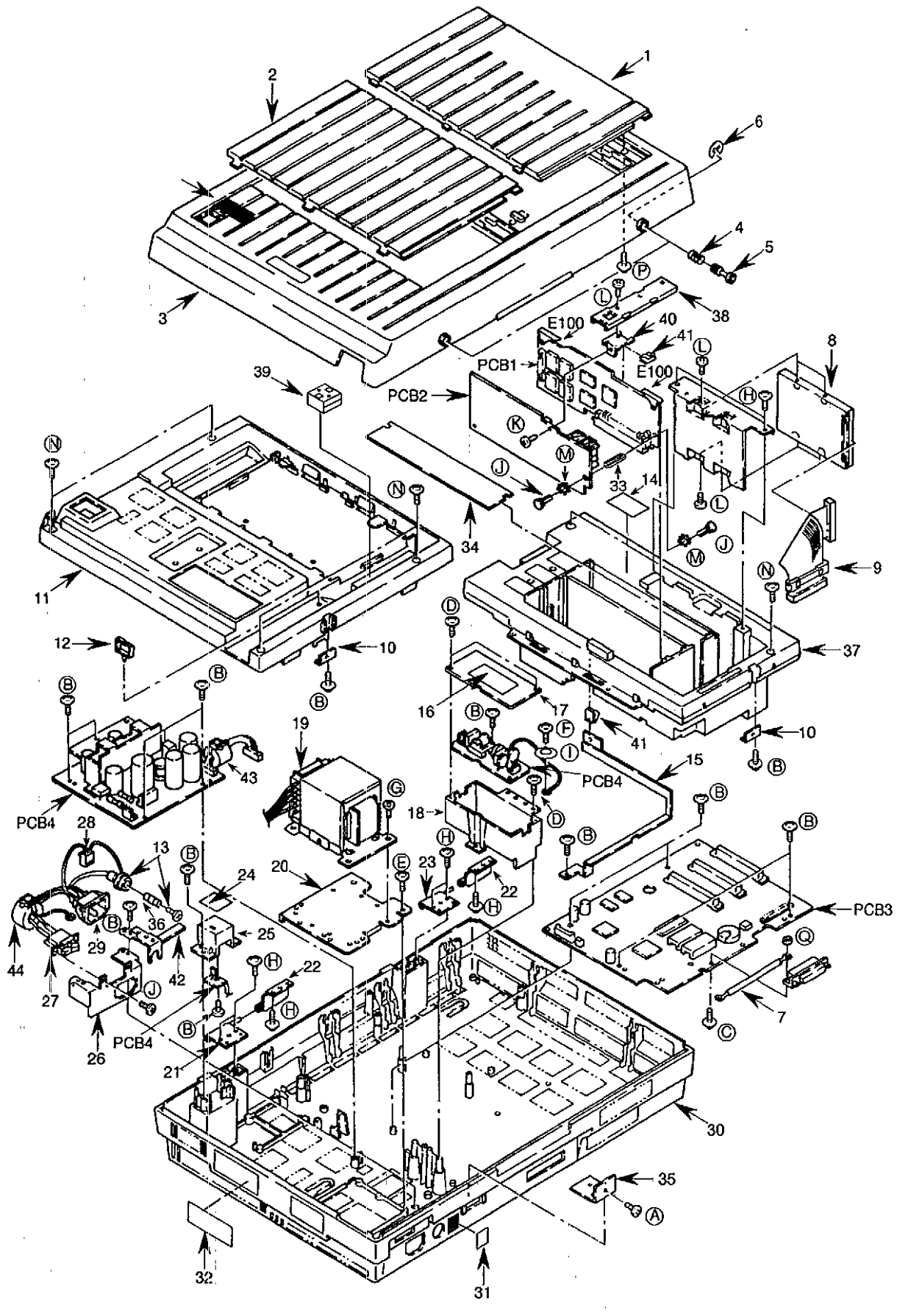


SCHEMATIC DIAGRAM (AC/DC POWER AND LED)

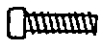


MEMO

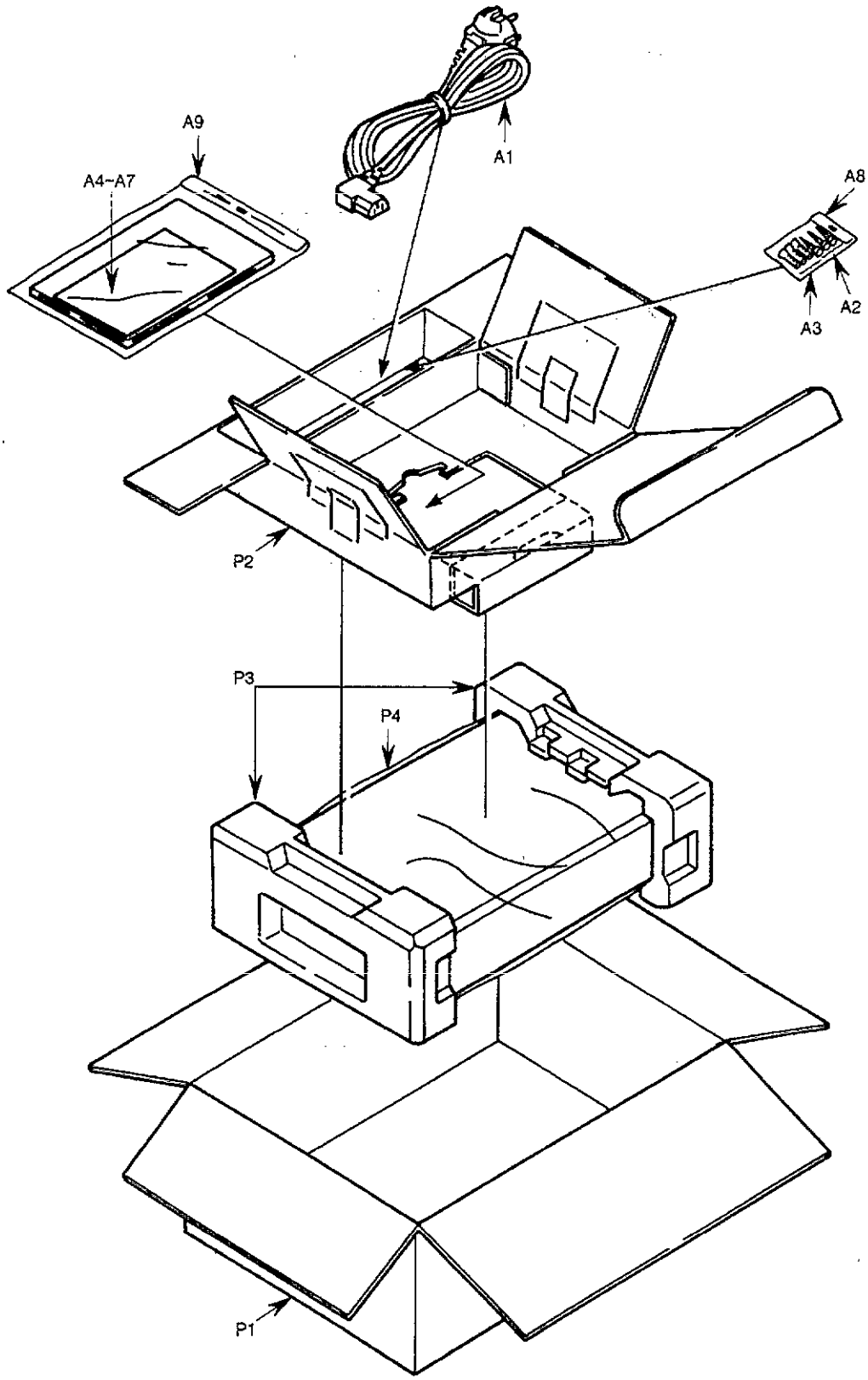
CABINET AND ELECTRICAL PARTS LOCATION



ACTUAL SIZE OF SCREWS AND WASHER

Ref. No.	Part No.	Figure
Ⓐ	XSN4D8FN	
Ⓑ	XTW3+S10P	
Ⓒ	XYN3+C10	
Ⓓ	XTW3+S14P	
Ⓔ	XTW4+12S	
Ⓕ	XYN4+C8	
Ⓖ	XYN4+F8	
Ⓗ	XTB3+10GFN	
Ⓘ	XWC4B	
Ⓙ	XYN3+C6	
Ⓚ	XYN3+F6FU	
Ⓛ	XYN3+6CFN	
Ⓜ	XWC3B	
Ⓝ	XTW3+S16M	
Ⓟ	XTW3+W8F	
Ⓠ	PQHE7011Z	

ACCESSORIES AND PACKING MATERIALS



This replacement parts list is for KX-TVP100E only. Refer to the simplified manual (cover) for other areas.

REPLACEMENT PARTS LIST

Model KX-TVP100E

Notes:

1. The marking (RTL) indicates that the Retention Time is limited for this item. After the discontinuation of this assembly in production, the item will continue to be available for a specific period of time. The retention period of availability is dependent on the type of assembly, and in accordance with the laws governing part and product retention. After the end of this period, the assembly will no longer be available.
2. Important safety notice.
   Components identified by the ⚠ mark special characteristics important for safety.
   When replacing any of these components, use only manufacturer's specified parts.
3. The S mark indicates service standard parts and may differ from production parts.
4. RESISTORS & CAPACITORS
   Unless otherwise specified.
   All resistors are in ohms (Ω) k=1000Ω, M=1000kΩ
   All capacitors are in MICRO FARADS(μF) P= μμF
   *Type &Wattage of Resistor
   Type

ERC:Solid	ERX:Metal Film	PQRD:Carbon
ERD:Carbon	ERG:Metal Oxide	PQRQ:Fuse
PQ4R:Chip	ERO:Metal Film	ERF:Wire Wound

Wattage

10,16,18:1/8W	14,25,S2:1/4W	12,50,S1:1/2W	1:1W	2:2W	5:5W

*Type & Voltage of Capacitor
Type

ECFD:Semi-Conductor	ECCD,ECKD,PQCBC,PQVP : Ceramic
ECQS:Styrol	ECQM,ECQV,ECQE,ECQU,ECQB : Polyester
PQCBX,ECUV:Chip	ECEA,ECSZ,ECOS : Electrolytic
ECMS:Mica	ECQP : Polypropylene

Voltage

ECQ Type	ECQG ECQV Type	ECSZ Type	Others	
1H: 50V	05: 50V	OF:3.15V	OJ :6.3V	1V :35V
2A:100V	1:100V	1A:10V	1A :10V	50,1H:50V
2E:250V	2:200V	1V:35V	1C :16V	1J :63V
2H:500V		OJ:6.3V	1E,25:25V	2A :100V

Ref. No.	Part No.	Part Name & Description	Pcs
		CABINET & ELECTRICAL PARTS	
1	PQKV10006T1	COVER-A FRONT	1
2	PQKV10005Y1	COVER-B FRONT	1
3	PQKE10021P1	COVER	1
4	PQUS141Z	SPRING	2
5	PQHD10011Z	SCREW	2
6	XUC3VW	RETAINING RING	2
7	PQWW1005Z	FG FOUTE CABLE	1
8	PSWEVP100E	H.D.D. ASS'Y	1
9	PQJS44Q77Y	CONNECTOR, 44P	1
10	PQMH10008Z	ANGLE	2
11	PQKF10066V1	INSIDE COVER	1
12	PQHR118Z	CLAMPER	1
13	PQJV5Z	FUSE BOX ⚠	1
14	PQQT10918Z	WARNING LABEL	1
15	PQMC10101Z	FG ROUTE PLATE	1
16	PQQT4181Z	WARNING LABEL	1
17	PQHR10173Z	UPPER COVER, POWER CARD	1
18	PQHR10174Y	LOWER COVER, POWER CARD	1
19	PSLT5M9A12A	POWER TRANSFORMER ⚠	1
20	PQMH10112Z	CHASSIS, TRANSFORMER	1
21	PQMH10010Y	HINGE-A	1
22	PQMH10009Z	HINGE-B	2
23	PQMH10010Z	HINGE-C	1
24	PQGP10009Z1	PANEL, LED	1
25	PQGG10009Z1	GRILLE, LED	1
26	PQMH10027Y	CHASSIS, POWER SWITCH	1
27	EST15304V	CHASSIS, POWER SWITCH ⚠	1
28	PQJS02R37Z	CONNECTOR, 2P	1
29	PQJP3A3Z	AC INLET ⚠	1
30	PQKM10086L1	LOWER CABINET	1
31	PSQT1169Z	FUSE LABEL	1
32	PSGT1186Z	NAME PLATE ⚠	1
33	PSHE1010Z	SPACER	1
34	PQHR10394Z	COVER	1
35	PQMC10059Y	FG PLATE	1
36	XBA2C063TB0L	FUSE ⚠	1
37	PQKE10037W1	PARTING PLATE	1
38	PQMD10058Z	CHASSIS, CO CARD	1
39	PSLB5F1	FERRITE CORE	1
40	PQMH10151Z	ANGLE	1
41	PQMH10152Z	SPRING	3
42	PSMH1043Z	ANGLE	1
43	PQLB5D2	FERRITE CORE	1
44	PQLB5F1	FERRITE CORE	1
		ACCESSORIES AND PACKING MATERIALS	
A1	PQJA10045Z	POWER CORD ⚠	1
A2	PQHE5008Z	MOUNTING BRACKET(SCREW)	3
A3	PQHE10Z	MOUNTING BRACKET(PLUG)	3
A4	PSQX1101Z	INSTALLATION MANUAL	1
A5	PQQX10552W	TEMPLATE	1
A6	PSQX1102Z	INSTRUCTION BOOK	1
A7	PQQX10970Y	CARD, REMOTE	10
A8	XZB05X08A03	PROTECTION COVER (MOUNT BRACKET)	1
A9	XZB25X34A04	PROTECTION COVER(MANUALS)	1
P1	PSPK1141Z	PACKING CASE	1
P2	PQPN10191Y	ACCESSORY BOX	1
P3	PQPN10196Z	CUSHION	2
P4	PQPP10022Z	PROTECTION COVER (SET)	1
		DSP BOARD PARTS	
PCB1	PSWP1VP100E	DSP BOARD ASS'Y (RTL)	1
		(ICs)	
IC101	PQVIPD656214	IC	1
IC102,103	PQVISN7L244S	IC	2
IC104	PQVISN7L245S	IC	1
IC105	PQVISN7L241M	IC S	1
IC106	PQVISN7L126A	IC	1
IC107A/108A	PSWI1VP100E	IC	1
IC107B/108B	PSWI1VP100E	IC	1
IC109A,109B	PSVI8C025APJ	IC	2
		(TRANSISTORS)	
Q100	PQVTDTC143E	TRANSISTOR(SI)	1

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Ref. No.	Part No.	Part Name & Description	Pcs
		(CONNECTORS)	
CN101	PQJP50S33Z	CONNECTOR, 50p	1
CN102	PQJP30A86Z	CONNECTOR, 30p	1
		(CAPACITORS)	
C100,101	ECUV1H102KBV	0.001	2
C102,103	ECUV1H120JCV	12p	2
C104,105	ECUV1H104ZFV	0.1	2
C114A, 114B	ECUV1H102KBV	0.001	2
C115A, 115B	ECUV1H104ZFV	0.1	2
C116A, 116B	PQCUV1H223KB	0.022	2
C117A, 117B	ECUV1C391JCV	390p	2
C118A, 118B	ECUV1H104ZFV	0.1	2
C119A, 119B	PQCUV1H105JC	1 S	2
C120A, 120B	ECUV1H104ZFV	0.1	2
C121A, 121B	ECUV1H104ZFV	0.1	2
C122A, 122B	ECUV1H104ZFV	0.1	2
C123A, 123B	ECUV1H104ZFV	0.1	2
C180	ECEA1AKS221	220	1
C181-184	PQCUV1H105JC	1 S	4
C185-189	ECUV1H104ZFV	0.1	5
		(COILS)	
L104A,104B	PQLQRIRS121	CHOKE COIL	2
L105A,105B	PQLQRIRS121	CHOKE COIL	2
L106A,106B	PQLQRIRS121	CHOKE COIL	2
L110,111,112	PQLQRIRS121	CHOKE COIL	3
		(RESISTORS)	
R100,102	ERJ3GEYJ330	33	2
R105, 106	ERJ3GEYJ473	47k	2
R108	ERJ3GEYJ221	220	1
R110,111	ERJ3GEYJ330	33	2
R113,114	ERJ3GEYJ330	33	2
R115A, 115B	ERJ3GEYJ473	47k	2
R116A, 116B	ERJ3GEYJ272	2.7k	2
R117A, 117B	ERJ3GEYJ473	47k	2
R118A, 118B	ERJ3GEYJ473	47k	2
R119A, 119B	ERJ3GEYJ473	47k	2
R120A, 120B	ERJ3GEYJ473	47k	2
R121A, 121B	ERJ3GEYJ473	47k	2
R122A, 122B	ERJ3GEYJ473	47k	2
R123A, 123B	ERJ3GEYJ473	47k	2
R124A, 124B	ERJ3GEYJ473	47k	2
R125A, 125B	ERJ3GEYJ473	47k	2
R126A, 126B	ERJ3GEYJ473	47k	2
R127A, 127B	ERJ3GEYJ473	47k	2
R128A, 128B	ERJ3GEYJ473	47k	2
R129A, 129B	ERJ3GEYJ473	47k	2
R130A, 130B	ERJ3GEYJ473	47k	2
R131A, 131B	ERJ3GEYJ473	47k	2
R141	ERJ3GEYJ473	47k	1
R142A, 142B	ERJ3GEYJ473	47k	2
		(CRYSTAL OSCILLATOR)	
X100	PQVCJ16384N8	CRYSTAL OSCILLATOR	1
		(OTHERS)	
E100	PQHR10207Z	LEVER	2

Ref. No.	Part No.	Part Name & Description	Pcs
		CO BOARD PARTS	
PCB2	PSWP2VP100E	CO BOARD ASS'Y (RTL) ⚠	1
		(ICs)	
IC241A, 241B	PQVIMP58C20D	IC	2
IC242A, 242B	PQVINJM2058V	IC	2
IC243A, 243B	PQVITC4S66F	IC	2
IC244A, 244B	PQVITC4S66F	IC	2
IC261A	PQVINJM319V	IC	1
		(TRANSISTORS)	
Q200A,200B	PQVTDTC143E	TRANSISTOR(SI)	2
Q212	PQVTDTC143E	TRANSISTOR(SI)	1
Q213	PQVTDTA143EU	TRANSISTOR(SI)	1
Q261A, 261B	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q) ⚠	1
Q281A, 281B	2SD2040	TRANSISTOR(SI) ⚠	2
Q282A, 282B	2SA1627	TRANSISTOR(SI) ⚠	2
		(DIODES)	
D200A, 200B	MA4039	DIODE(SI)	2
D201A, 201B	MA4039	DIODE(SI)	2
D281A, 281B	PQVDS1ZB40F1	DIODE(SI) ⚠	2
D282A, 282B	PQVDHZS2B1	DIODE(SI) ⚠	2
		(CONNECTOR & JACK)	
CN201	PQJS30A53Z	CONNECTOR, 30p	1
CN291	PQJJ2T003Z	JACK, TEL	1
		(CAPACITORS)	
C201, 202	ECEA1AU221	220	2
C230A	PQCUV1H223KB	0.022	1
C231A, 231B	PQCUV1H223KB	0.022	2
C233A, 233B	PQCUV1H223KB	0.022	2
C234A	PQCUV1H223KB	0.022	1
C235A, 235B	PQCUV1H223KB	0.022	2
C237A	PQCUV1H223KB	0.022	1
C237B	ECUV1H223KBV	0.022	1
C241A, 241B	PQCUV1H682KB	0.0068	2
C242A, 242B	PQCUV1E104MD	0.1	2
C244A, 244B	PQCUV1H271JC	270p	2
C245A, 245B	PQCUV1H682KB	0.0068	2
C246A, 246B	PQCUV1E104MD	0.1	2
C247A, 247B	PQCUV1H101JC	100P	2
C248A, 248B	PQCUV1H101JC	100P	2
C249A, 249B	PQCUV1H101JC	100P	2
C250A, 250B	PQCUV1H223KB	0.022	2
C252A, 252B	PQCUV1C154KB	0.15	2
C254A, 254B	PQCUV1C154KB	0.15	2
C255A, 255B	PQCUV1H102J	0.001	2
C256A, 256B	PQCUV1H103KB	0.01	2
C257A, 257B	ECEA1HUR47	0.47	2
C261A, 262A	ECEA1HKS010	1	2
C263A, 264A	PQCUV1H680JC	68p	2
C265A, 266A	PQCUV1H101JC	100p	2
C267A, 268A	PQCUV1H470JC	47P	2
C269A	PQCUV1H223KB	0.022 S	1
C270A, 270B	PQCUV1H101JC	100p	2
C271A, 271B	ECUV1C105KB	1	2
C272A, 272B	PQCUV1H223KB	0.022 S	2
C281A, 281B	ECEA1HU4R7	4.7	2
C282A, 282B	ECEA1HU330	33	2
C283A, 283B	ECQE2E474KZ	0.47	2
C284A, 284B	ECKDKC222KB	0.0022 ⚠ S	2
		⚠	2
C291A, 292A	ECEA1HN4R7S	4.7	2

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Ref. No.	Part No.	Part Name & Description	Pcs
		(COILS)	
R200A,200B	PQ4R10XJ102	1k	2
R201A,201B	PQ4R10XJ152	1.5k	2
L201, 202	PQLQR1T2R2M	COIL	2
L210, 211	PQLQR1LT	COIL	2
L281A, 281B	PQLE106	COIL	2
L282A, 282B	PQLE106	COIL	2
L283A, 283B	PQLE106	COIL	2
L284A, 284B	PQLE106	COIL	2
L285A, 285B	PQLE106	COIL	2
L286A, 286B	PQLE106	COIL	2
L291A, 291B	PQLQR1LT	COIL	2
		(PHOTO ELECTRIC TRANSDUCERS)	
PC200A, 200B	PQVITLP627	PHOTO COUPLER	2
PC281A, 281B	PSVIPC817IK	PHOTO COUPLER ⚠S	2
PC282A, 282B	PQVITLP627	PHOTO COUPLER ⚠	2
PC283A, 283B	PSVIPC814IK	PHOTO COUPLER ⚠	2
		(RESISTORS)	
R202A,202B	ERDS2TJ101	100	2
R203A,203B	PQ4R10XJ101	100	2
R212-214	PQ4R10XJ000	0	2
R215, 216	PQ4R10XJ472	4.7k	2
R223,225,226	ERJ3GEYJ101	100	3
R227,229,230	PQ4R10XJ101	100	3
R231A, 231B	PQ4R10XF1203	120k	2
R232A, 232B	PQ4R10XF4702	47k	2
R233A, 233B	PQ4R10XF4702	47k	2
R234A, 234B	PQ4R10XF1203	120k	2
R235A, 235B	PQ4R10XF1003	100k	2
R241A, 241B	PQ4R10XF1203	120k	2
R242A, 242B	PQ4R10XF4702	47k	2
R243A, 243B	PQ4R10XF1003	100k	2
R244A, 244B	PQ4R10XJ274	270k	2
R245A, 245B	PQ4R10XJ394	390k	2
R246A, 246B	PQ4R10XF4702	47k	2
R247A, 247B	PQ4R10XF4702	47k	2
R248A, 248B	PQ4R10XF1003	100k	2
R249A, 249B	PQ4R10XF1003	100k	2
R250A, 250B	PQ4R10XF1151	1.15k	2
R251A, 251B	PQ4R10XF4700	470	2
R252A, 252B	PQ4R10XF1201	1.2k	2
R253A, 253B	PQ4R10XF5600	560	2
R254A, 254B	PQ4R10XF1201	1.2k	2
R255A, 255B	PQ4R10XF5600	560	2
R256A, 256B	PQ4R10XJ104	100k	2
R257A	PQ4R10XJ104	100k	1
R257B	ERJ3GEYJ104	100k	1
R259A,259B	PQ4R10XJ102	1k	2
R260A, 260B	PQ4R10XF1003	100k	2
R261A	PQ4R10XJ330	33	1
R262A	PQ4R10XJ330	33	1
R263A-272A	PQ4R10XJ472	4.7k	10
R273A	PQ4R10XJ821	820	1
R274A	PQ4R10XF8201	8.2k	1
R275A	PQ4R10XF1201	1.2k	1
R276A	PQ4R10XJ330	33	1
R277A	PQ4R10XJ330	33	1
R281A, 281B	ERDS2TJ822	8.2k	2
R282A, 282B	ERDS2TJ682	6.8k	2
R283A, 283B	ERDS2TJ390	39	2
R284A, 284B	ERDS2TJ472	4.7k	2
R285A, 285B	ERDS2TJ104	100k	2
R286A, 286B	PQRQ25VJ5R6	5.6	2
R287A, 287B	ERQN1VJ223	22k	2
R288A, 288B	ERDS2TJ122	1.2k	2
R291A	ERQS1VJ122	1.2k	1
R291A	PQRQ2VJ561	560	1

Ref. No.	Part No.	Part Name & Description	Pcs
		(RELAYS)	
RL200A,200B	AQV214SX	RELAY	2
		(VARISTORS)	
SA200,200B	PQVDT83A350X	VARISTOR (SURGE ABSORBER)	2
SA201,202	PSVDY08Z102B	VARISTOR (SURGE ABSORBER)	2
ZR281A, 281B	ERZC07DK820	VARISTOR ⚠S	2
ZR291A, 292A	ERZC07DK820	VARISTOR ⚠S	2
		(TRANSFORMERS)	
T281A, 281B	PQLT8E3A	TRANSFORMER ⚠	2
T291A	PQSLT9Z7A	TRANSFORMER ⚠	1
		CPU BOARD PARTS	
PCB3	PSWP3VP100E	CPU BOARD ASS'Y (RTL)	1
		(ICs)	
IC301	PQVI68301FCG	IC	1
IC302	PQVIPD656109	IC	1
IC303	PQVIMT8952BE	IC	1
IC304, 305	PQVIHM51480E	IC S	2
IC306, 307	PSWI2VP100E	IC	1
IC308	PQVIMS6242BG	IC	1
IC310	PQVIPS520C	IC	1
IC311	PQVIDS14C232	IC	1
IC312, 313	PQVISN7L245S	IC	2
IC314-317	PQVISN7L244S	IC	4
IC318	PQVISN7L245S	IC	1
IC319	PQVISN7L244S	IC	1
		(TRANSISTORS)	
Q301	PQVTDTC143E	TRANSISTOR(SI)	1
		(DIODES)	
D300	MA723	DIODE(SI)	1
D301	MA742	DIODE(SI)	1
		(BATTERY)	
BATT301	CR23541GUF	LITHIUM BATTERY	1
		(CONNECTORS & JACK)	
CN301	PQJP44B15Z	CONNECTOR, 44p	1
CN302-304	PQJS50S33Z	CONNECTOR, 50p	3
CN305	PQJP8D94Z	CONNECTOR, 8p	1
CN306	PQJP2D70Z	CONNECTOR, 2p	1
CN307	PQJS25P31Z	SOCKET(RS-232C)	1
		(CAPACITORS)	
C3A1	PQCUV1H221JC	220p	1
C3A2	PQCUV1H102J	0.001	1
C3A3	PQCUV1H680JC	68p	1
C3A4-3A6	PQCUV1H221JC	220p	3
C3A7-3A9	PQCUV1H105JC	1	3
C3B1	PQCUV1H105JC	1	1
C3B2-3B4	PQCUV1H104ZF	0.1	3
C3B5	PQCUV1H105JC	1	1
C3B6, 3B7	PQCUV1H221JC	220p	2
C301, 302	PQCUV1H102J	0.001	2
C305	ERJ3GEYOR00	0	1
C306	ECUV1H680JCV	68p	1
C308	PQCUV1H102J	0.001	1
C309	ECUV1H104ZFV	0.1	1
C310	PQCUV1H104ZF	0.1	1
C311	ECUV1H104ZFV	0.1	1

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Ref. No.	Part No.	Part Name & Description		Pcs
C312	PQCUV1H104ZF	0.1		1
C313	ECUV1H104ZFV	0.1		1
C314	PQCUV1H104ZF	0.1		1
C315	ECUV1H104ZFV	0.1		1
C316	PQCUV1H102J	0.001		1
C317, 318	PQCUV1H104ZF	0.1		2
C319	PQCUV1H200JC	20p		1
C320	PQCUV1H200JC	20p		1
C322	ECEA1VKS4R7	4.7	S	1
C324	ECEA1CKS100	10		1
C325-328	ECEA1VKS4R7	4.7	S	4
C329	PQCUV1H5R0CC	5		1
C330	PQCUV1H5R0CC	5		1
C370	ECEA1EU101	100		1
C371-373	ECEA1EU331	330		3
C380	PQCUV1H104ZF	0.1		1
C381	ECUV1H104ZFV	0.1		1
C382-387	PQCUV1H104ZF	0.1		6
C388	ECUV1H102KBV	0.001		1
C389	PQCUV1H104ZF	0.1		1
C390-396	PQCUV1H105JC	1		7
C397	PQCUV1H221JC	220p		1
C398	PQCUV1H104ZF	0.1		1
C399	PQCUV1H221JC	220p		1
		(CERAMIC FILTER)		
L303-306	PQVFTU50MT	CERAMIC FILTER		4
		(RESISTORS)		
R3AA-3AF	ERJ3GEYJ473	47k		6
R3A0-3A9	ERJ3GEYJ473	47k		10
R3B0-3B7	PQ4R10XJ103	10k		8
R3C0-3C3	PQ4R10XJ472	4.7k		4
R3D0-3D9	PQ4R10XJ330	33		10
R3E0-3E8	PQ4R10XJ330	33		9
R3E9	ERJ3GEYJ330	33		1
R3F0	ERJ3GEYJ330	33		1
R3F1	PQ4R10XJ330	33		1
R3F2	ERJ3GEYJ330	33		1
R3F3, 3F4	PQ4R10XJ101	100		2
R3F5, 3F6	ERJ3GEYJ330	33		2
R3F7-3F9	PQ4R10XJ101	100		3
R3G0-3G9	PQ4R10XJ101	100		10
R3H0-3H5	PQ4R10XJ101	100		6
R3H6	PQ4R10XJ103	10k		1
R3H7	ERJ3GEYJ103	10k		1
R3H8, 3H9	PQ4R10XJ103	10k		2
R3J0	ERJ3GEYJ103	10k		1
R3J1-3J9	PQ4R10XJ103	10k		9
R3K0-3K9	PQ4R10XJ103	10k		10
R3L0	PQ4R10XJ103	10k		1
R3L1, 3L2	ERJ3GEYJ103	10k		2
R3L3	PQ4R10XJ103	10k		1
R3L4	ERJ3GEYJ103	10k		1
R3L5	ERJ3GEYJ152	1.5k		1
R3L7	PQLQR1K7	COIL		1
R3L9	ERJ3GEYJ330	33		1
R3M0	ERJ3GEYJ330	33		1
R3M1	PQ4R10XJ330	33		1
R3N0-3N4	ERJ3GEYJ103	10k		5
R3N5-3N8	PQ4R10XJ103	10k		4
R3N9	ERJ3GEYJ103	10k		1
R301, 302	PQ4R10XJ330	33		2
R303, 305	PQ4R10XJ472	4.7k		2
R306	PQ4R10XJ103	10k		1
R307, 308	PQ4R10XJ472	4.7k		2

Ref. No.	Part No.	Value, Part Name & Description		Pcs
R310	PQ4R10XJ101	100		1
R311	PQ4R10XJ000	0		1
R312	PQ4R10XJ101	100		1
R313-319	PQ4R10XJ330	33		7
R320	PQ4R10XJ472	4.7k		1
R321	ERJ3GEY0R00	0		1
R323	ERJ3GEY0R00	0		1
R324	PQLQR1RS121	COIL		1
R325	PQLQR1RS121	COIL		1
R326	ERJ3GEY0R00	0		1
R327	PQ4R10XJ000	0		1
R329	PQLQR1LT	COIL		1
R331, 332	ERJ3GEYJ473	47k		2
R333	PQ4R10XJ473	47k		1
R336-339	PQ4R10XJ473	47k		4
R342	PQ4R10XJ103	10k		1
R344, 345	PQ4R10XJ000	0		2
R346	ERJ3GEY0R00	0		1
R360	PQ4R10XJ184	180k		1
R362	PQ4R10XJ330	33		1
R363-369	PQ4R10XJ101	100		7
R370	PQ4R10XJ103	10k		1
R372	PQ4R10XJ473	47k		1
R376	PQ4R10XJ103	10k		1
		(SWITCH)		
SW301	PQSR10A101Z	SWITCH		1
		(CRYSTAL OSCILLATORS)		
X300	PQVCL3276N6Z	CRYSTAL OSCILLATOR		1
X301	PQVCJ2457N3Z	CRYSTAL OSCILLATOR		1

AC/DC POWER & LED BOARD PARTS

PCB4	PSWP4VP100E	AC/DC POWER & LED BOARD ASS'Y (RTL)	⚠	1
		(ICs)		
IC400	PQVIHLD05003	IC		1
IC401	AN7805	IC		1
		(TRANSISTORS)		
Q1	2SB945	TRANSISTOR(SI)		1
Q2	DTC143EA	TRANSISTOR(SI)		1
Q5	2SA933	TRANSISTOR(SI)		1
		(DIODES)		
D400	PQVDD3SBA40S	DIODE(SI)		1
D401	PQVD2B4B41	DIODE(SI)		1
D402, 403	PQVDS5688G	DIODE(SI)		2
D404	MA4056	DIODE(SI)		1
D405	MA4047	DIODE(SI)		1
D406	PQVDD5S4M	DIODE(SI)		1
D407, 408	PQVDS5688G	DIODE(SI)		2
D409	PQVDSB340	DIODE(SI)	S	1
D410	PQVDD5S4M	DIODE(SI)		1
D801	LN242RP	LED		1

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Ref. No.	Part No.	Value, Part Name & Description	Pcs
		(FUSES)	
F400	XBA2C31TB0L	FUSE (for KX-TVP100BX) ⚠	1
F401	XBA2C12TB0L	FUSE (for KX-TVP100BX) ⚠	1
		(CONNECTORS)	
CN400	PQJP4D97Z	CONNECTOR, 4p	1
CN401	PQJS08Q04Z	CONNECTOR, 8p	1
CN450, 451	PQJP2D98Z	CONNECTOR, 2p	2
CN801	PQJS02R48Y	CONNECTOR, 2p	1
		(CAPACITORS)	
C400	ECET25S103SW	10000	1
C401	ECEA1EGE222	2200	1
C402, 403	ECQV1H104JZ	0.1	2
C404, 405	ECEA1EGE102	1000	2
C406	ECEA1AGE102	1000	1
C407	ECQV1H104JZ	0.1	1
C409	ECEA1AGE102	1000	1
C450, 451	ECKDKC472KB	0.0047 ⚠	2
C452, 453	ECQU2A473MN	0.047 ⚠	2
		(COILS)	
L400	PQLE72	COIL	1
L401	PQLE94	COIL	1
L450	ELF18D270D	COIL ⚠	1
		(RESISTORS)	
R400	ERG1SJ471	470	1
R401	ERDS2TJ102	1k	1
R402	ERG2SJ681	680	1
R403	PQRF2TLKR05	0.05	1
R404	ERDS2TJ331	330	1
R405	ERDS2TJ102	1k	1
R406, 407	ERDS2TJ471	470	2
R408	ERDS2TJ102	1k	1
R410	ERDS2TJ222	2.2k	1
R411	ERDS2TJ102	1k	1
R412-414	ERDS2TJ472	4.7k	3
R415	ERDS2TJ470	47	1
R416	ERF5TK1R5	1.5	1
R801	ERDS2TJ471	470	1
		(THYRISTORS)	
SCR400	PQVD03P2M	THYRISTOR	1
SC400-402	EECA0EL106	THYRISTOR	3
		(VARIABLE RESISTOR)	
VR400	EVNDXAA03B53	SEMI-FIXED RESISTOR, 5k	1
		(VARISTOR)	
ZNR450	ERZC14DK751U	VARISTOR ⚠	1

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